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## Process simulation for advanced stress and junction engineering

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**<https://cel.hal.science/cel-00667574v1>**

Submitted on 7 Feb 2012 (v1), last revised 8 Feb 2012 (v2)

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# ESSDERC/ESSCIRC Tutorial 2008: Characterisation for the nanoelectric era

## Process simulation for advanced stress and junction engineering

*Christophe Krzeminski and Evelyne Lampin*

*Email: [christophe.krzeminski@isen.fr](mailto:christophe.krzeminski@isen.fr)*

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59652 Villeneuve d'Ascq

France



# Tutorial objectives

*“Process simulation for advanced stress and junction engineering”*

» Large topic and only 45 minutes !

» and 53 slides

» Why Simulation in a characterisation tutorial ?

» Complementary...

» Not a so good idea to go deeply in the modeling aspect

» Overview of the field: the challenge (Part I), status (Part II), progress (Part III & IV) and perspectives (Part V)

» No equation

# Outline

Part I: Introduction: Challenge and solution for downscaling

Part II: Process simulation ?

Part III: Recent progress in the modeling of stress

Part IV: Recent progress in the modeling of junction engineering

Part V: Perspectives in Atomistic TCAD: towards some atomistic experiment ?

## Part I Introduction: Challenge and solution for downscaling

# Downscaling (→ 90 nm)

26

IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 18, NO. 1, FEBRUARY 2005

## In Search of “Forever,” Continued Transistor Scaling One New Material at a Time

Scott E. Thompson, *Senior Member, IEEE*, Robert S. Chau, *Senior Member, IEEE*, Tahir Ghani, Kaizad Mistry, Sunit Tyagi, *Member, IEEE*, and Mark T. Bohr, *Fellow, IEEE*

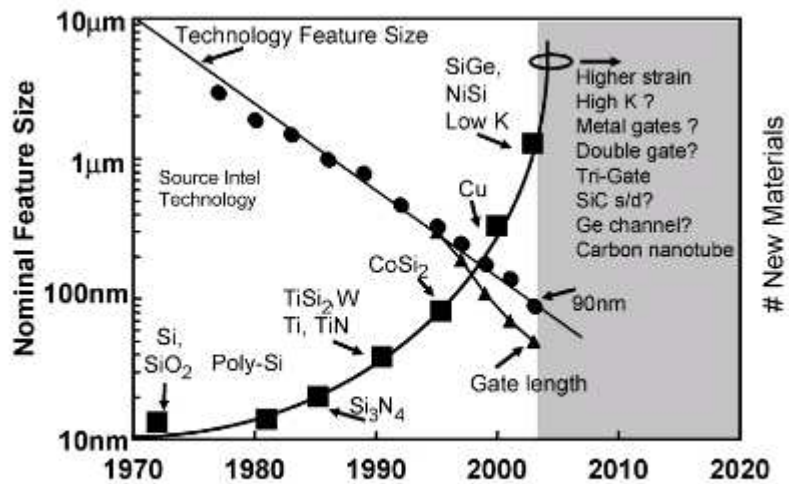
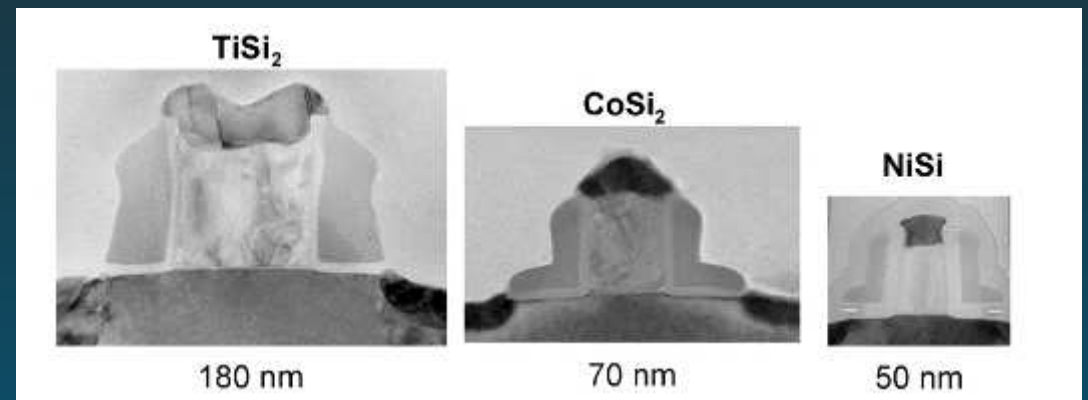


Fig. 2. Feature size and new materials versus year.



*S. E. Thompson et al., IEEE Trans. On Semiconductor Manufacturing, Vol. 18, n°1, 2005*

# Downscaling (→ 90 nm)

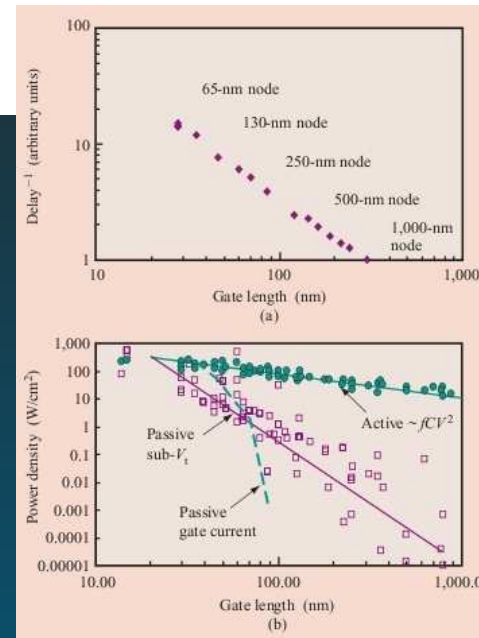
## Silicon CMOS devices beyond scaling

To a large extent, scaling was not seriously challenged in the past. However, a closer look reveals that early signs of scaling limits were seen in high-performance devices in recent technology nodes. To obtain the projected performance gain of 30% per generation, device designers have been forced to relax the device subthreshold leakage continuously from one to several nA/μm for the 250-nm node to hundreds of nA/μm for the 65-nm node. Consequently, passive power density is now a significant portion of the power budget of a high-speed microprocessor.

W. Haensch  
E. J. Nowak  
R. H. Dennard  
P. M. Solomon  
A. Bryant  
O. H. Dokumaci  
A. Kumar  
X. Wang  
J. B. Johnson  
M. V. Fischetti

**Table 1** Relationships for constant-field scaling and for generalized field scaling.  $\alpha$  is the scaling factor for dimensions, and  $E = V/\alpha$  is the normalized electric field.

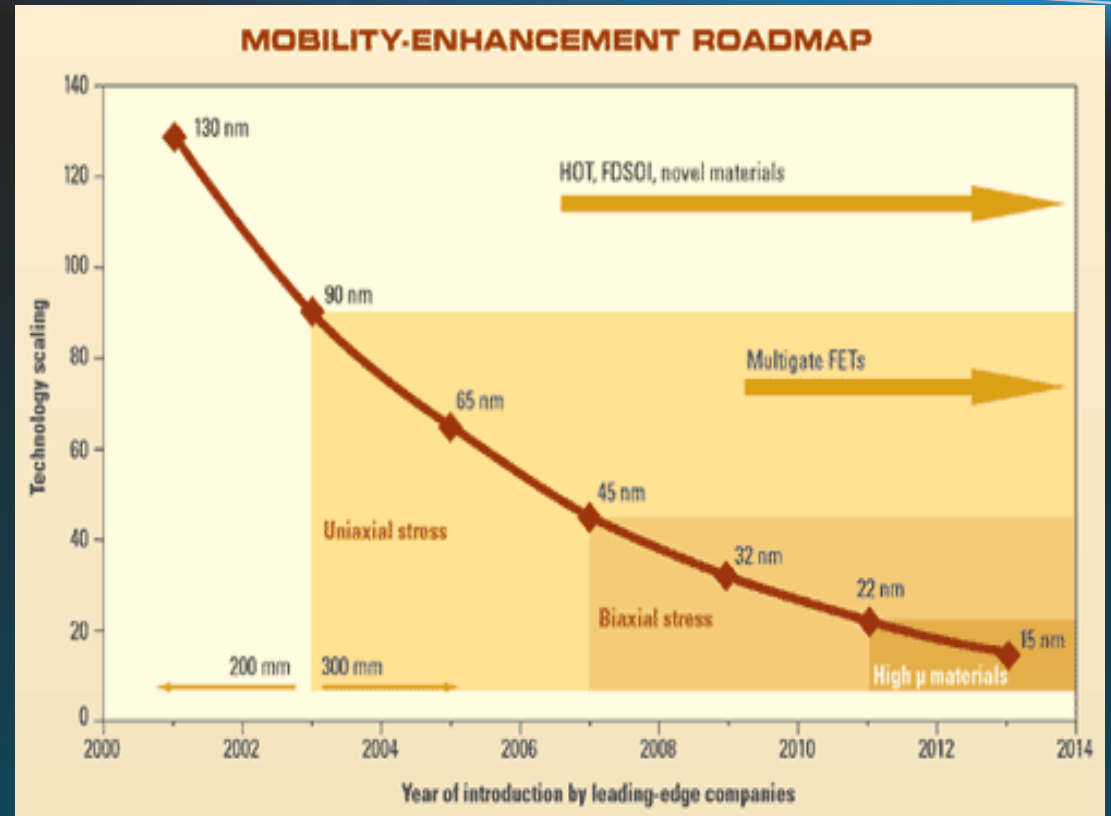
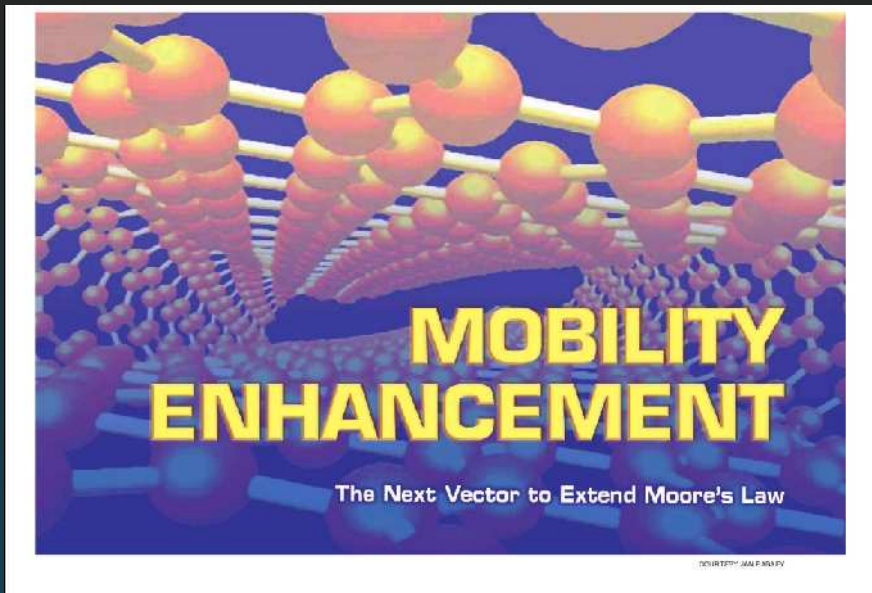
| Parameter  | Constant-field scaling | Generalized field scaling |
|--|------------------------|---------------------------|
| Physical dimensions, $L, W, T_{ox}$ , wire pitch | $1/\alpha$             | $1/\alpha$                |
| Body doping concentration                        | $\alpha$               | $E/\alpha$                |
| Voltage  | $1/\alpha$             | $E/\alpha$                |
| Circuit density                                  | $1/\alpha^2$           | $1/\alpha^2$              |
| Capacitance per circuit                          | $1/\alpha$             | $1/\alpha$                |
| Circuit speed                                    | $\alpha$               | $\alpha$ (goal)           |
| Circuit power                                    | $1/\alpha^2$           | $E^2/\alpha^2$            |
| Power density                                    | 1                      | $E^2$                     |
| Power-delay product (energy per operation)       | $1/\alpha^2$           | $E^2/\alpha^3$            |



W. Haensch et al., IBM J. Res&Dev, Vol. 50, n°45, 2006

# Stress Engineering approach

- (90nm → ?)



Mohta et al., IEEE Circuits and Magazine 2005

L. Peters, "Options Narrow at 45nm", Semiconductor International, 2006

Main idea: Strain engineering for enhanced mobility and drive current

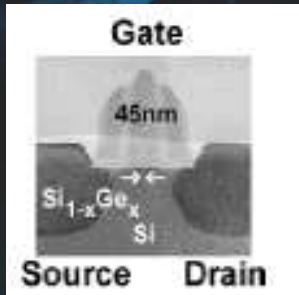


# Uniaxial stress techniques

PMOS

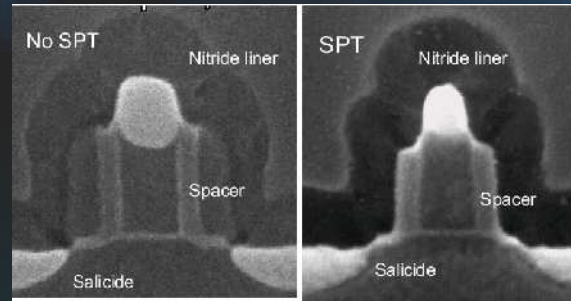
NMOS

## SiGe stressor (eSiGe)



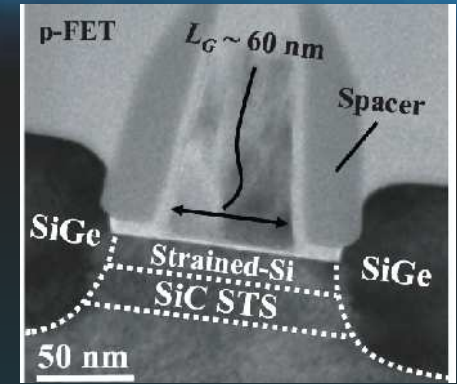
T. Ghani et al., IEDM 2003

## Stress Proximity Technique (SPT)



X. Chen et al., VLSI 2006

## Strain Transfer Structure (STS)



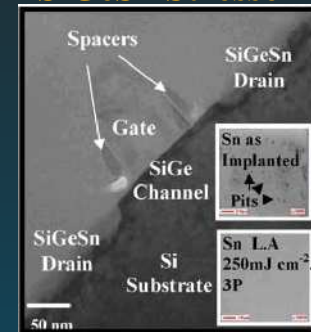
H. S. Ang et al., VLSI 2007

## Dual Stress Liner (DSL)



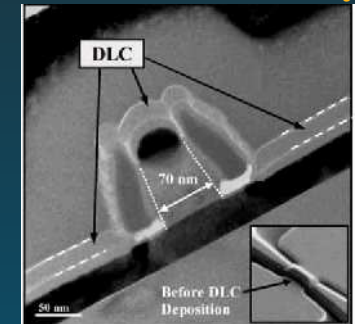
H. S. Yang et al., IEDM 2004

## SiGeSn Stressor



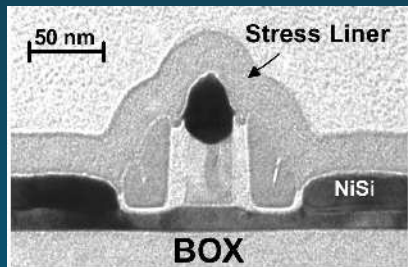
Wang, IEDM 2007

## Diamond Like Carbon layer (DLC)



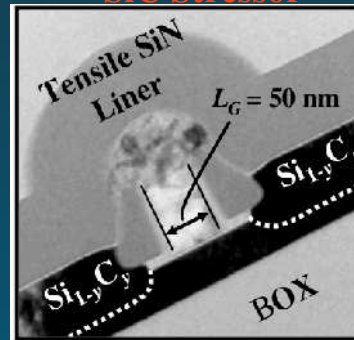
Tan, IEDM 2007

## Stress Memorization (SMT)



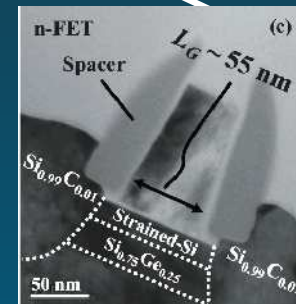
V. Singh et al., IEDM 2005

## SiC Stressor



Yeo, Semicond. Sci. Tech. 2007

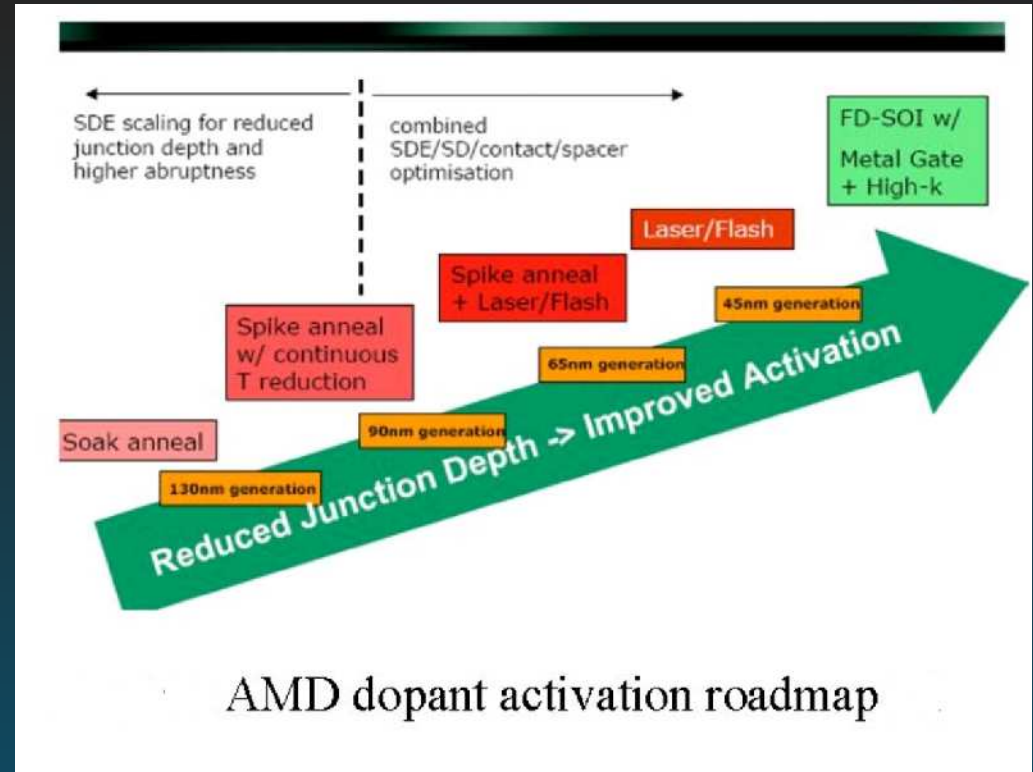
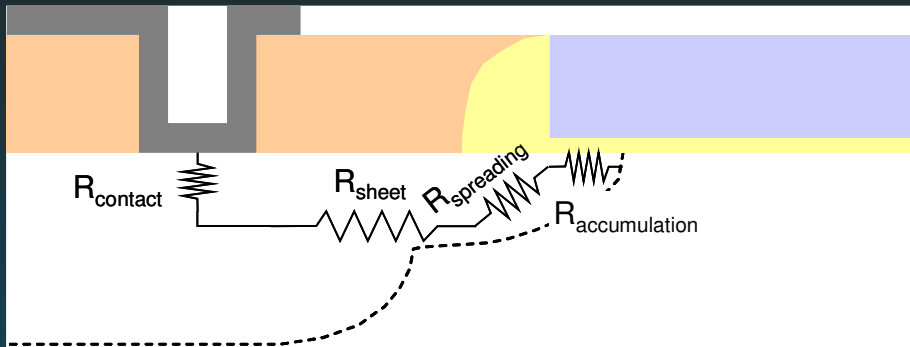
## Strain Transfer Structure (STS)



H. S. Ang et al., VLSI 2007

Level of stress in the channel

# Junction optimisation



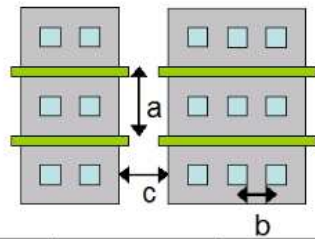
$R_{\text{Sheet}}$ : Conductivity of high doped region  
High activation: complex techniques

J. O. Borland, « 32 nm NODE USJ Implant & Annealing, RTP 2007

# Challenges for 32 & 22 nm

## Challenges and Opportunities for High Performance 32 nm CMOS Technology

J.W. Sleight, I. Lauer, O. Dokumaci, D. M. Fried, D. Guo, B. Haran, S. Narasimha, C. Sheraw, D. Singh, M. Steigerwalt, X. Wang, P. Oldiges, D. Sadana, C.Y. Sung, W. Haensch, and M. Khare  
 IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights NY 10598  
 sleight@us.ibm.com (914) 945-1876



|                   | 65 nm   | 45 nm      | 32 nm   |
|-------------------|---------|------------|---------|
| (a) Gate pitch    | ~250 nm | 180-190 nm | ~130 nm |
| (b) Contact Pitch | 195 nm  | 140-144 nm | ~100 nm |
| (c) N/P Spacing   | ~130 nm | ~102 nm    | ~70 nm  |

Fig. 1: Selected critical dimensions for different technology nodes.

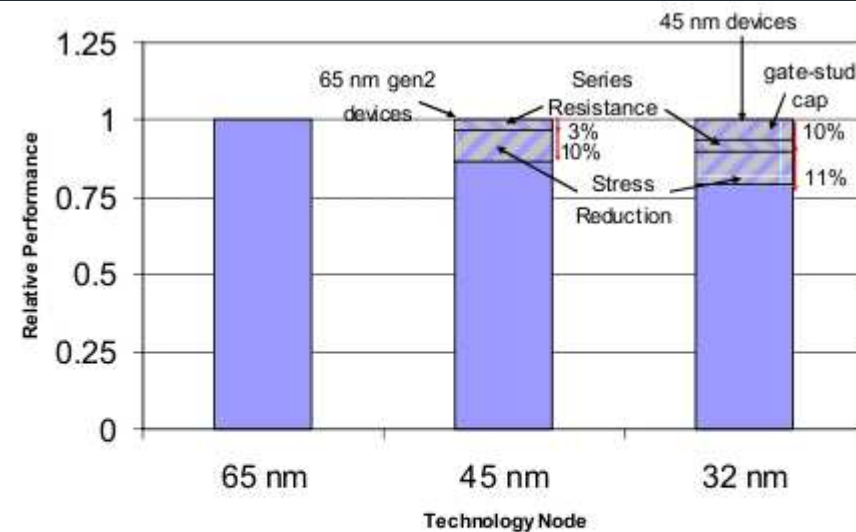


Fig. 2: Performance loss associated with pitch scaling for the 45 nm and 32 nm nodes. The performance loss associated with parasitics and stress loss is likely exacerbated at the 32 nm node.

J. W. Sleight et al., IEDM Tech. Dig., 2006

# Challenges for 32 nm

- Scalability:
    - -11% stress reduction compared to 65nm (decreasing gate pitch) [Sleight06]
    - ITRS Junction target (extension depth, abruptness& sheet resistance) challenging
  - Yield:
    - ITRS[07] : integration of multiple sources of local and global stress
    - Not exceeding the local critical shear stress
  - Design
    - Pitch and layout dependent
    - *“Strain adds new challenges from a design perspective”* [Lammers08]
- TCAD have a role to play to provide key information (process => design)

# PART II: Process Simulation ?

# TCAD ?



ELSEVIER

Materials Science and Engineering B 124-125 (2005) 81-85



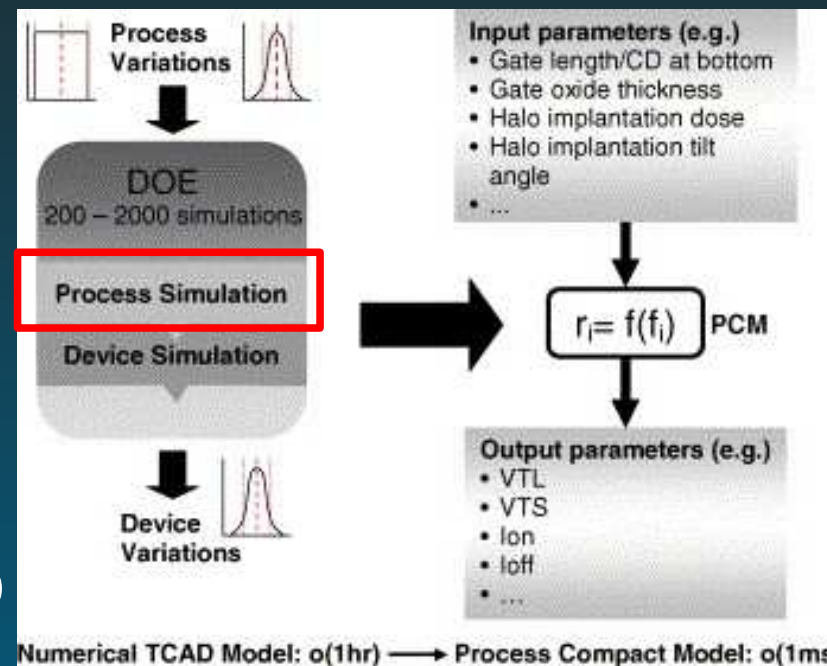
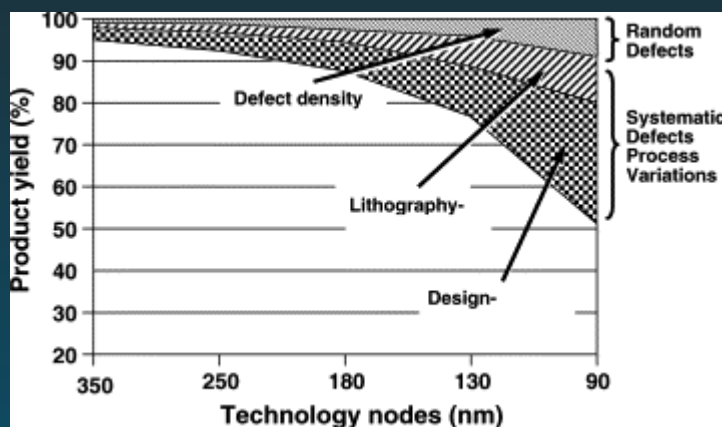
MATERIALS  
SCIENCE &  
ENGINEERING  
B

www.elsevier.com/locate/mseb

## Trends, demands and challenges in TCAD

Ingo Bork\*, Victor Moroz, Lars Bomholt, Dipu Pramanik

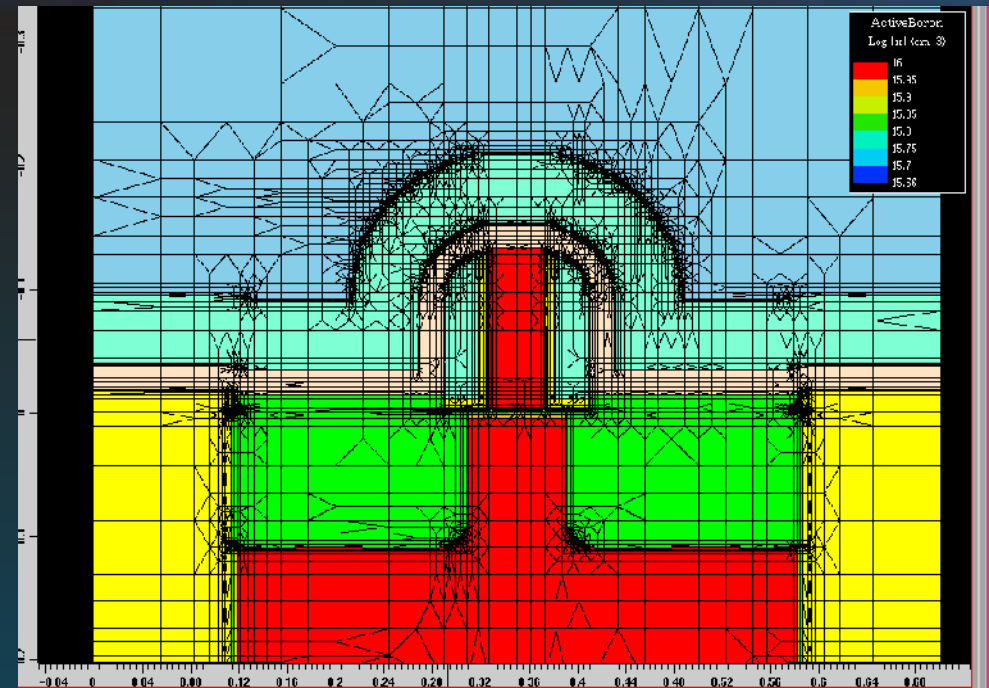
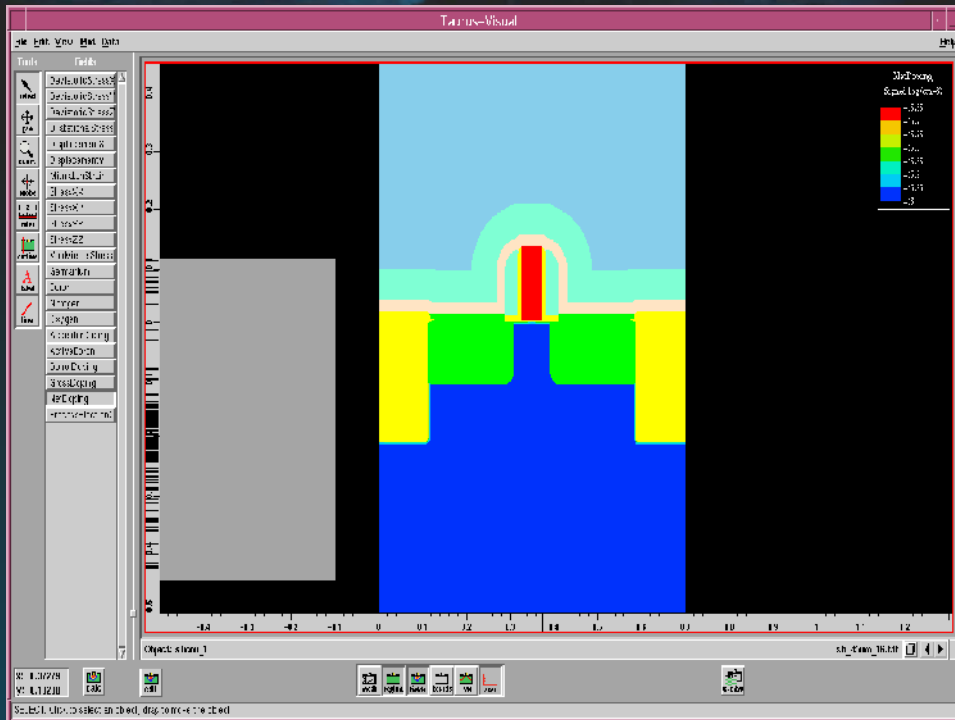
Synopsys, Inc., 700 E. Middlefield Rd., Mountain View, CA 94043, USA



## TCAD :

- ↘ Technology cost development (40% ITRS)
- ↗ Yield

# Process Simulation

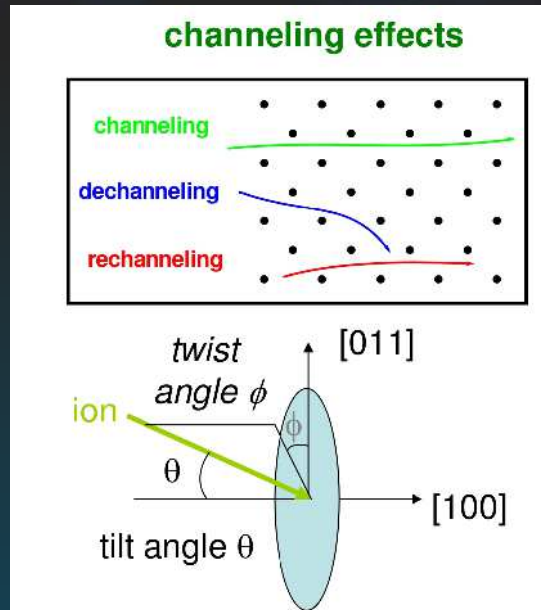


## Standard process simulation:

- Transistor Building (finite elements)
- Simulation of the various process step (implantation, diffusion, oxidation, silicidation)
- « Physical » modeling with partial differential equations (PDE)
- Knowledge of the various physical parameters (topology, dopant distribution, stress field) for electrical simulation

# Implantation modeling

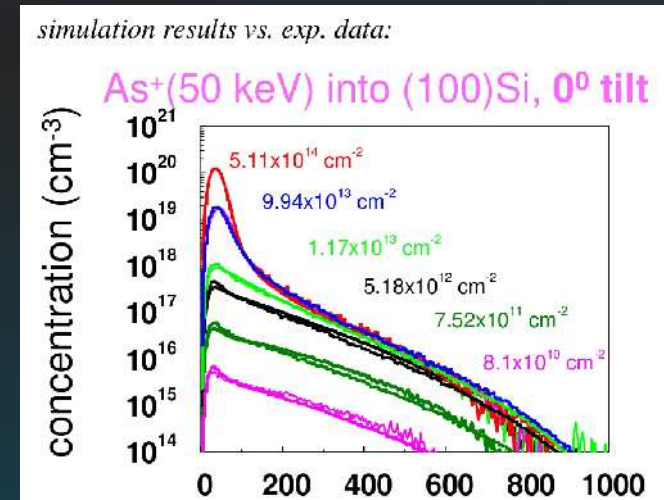
## Implantation modeling : Implant tables or Monte-Carlo Simulation



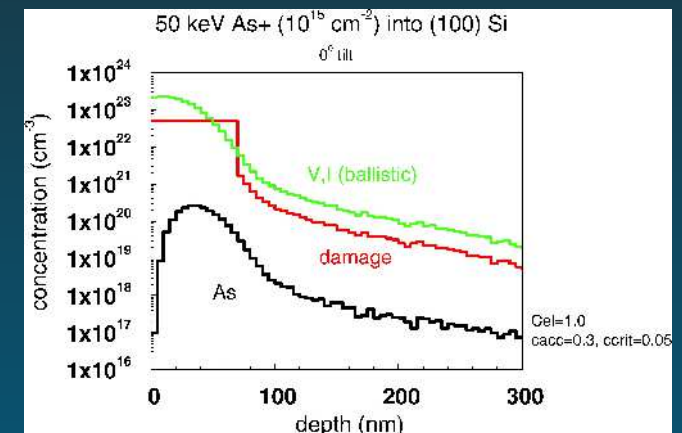
Series of consecutive binary collisions of the projectile with the lattice (BCA MC):

- Nuclear scattering (Coulomb pair potential)
- Semi empirical model for the electronic energy loss of particles
- Phenomenological models for damage probability

*M. Posselt, private communication*



Range distribution of implanted ions

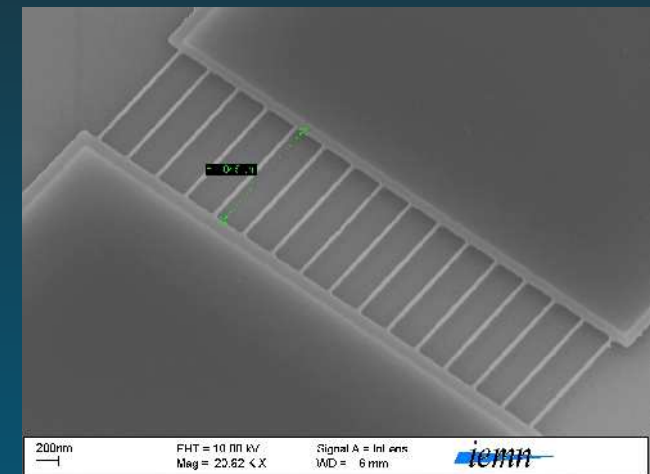
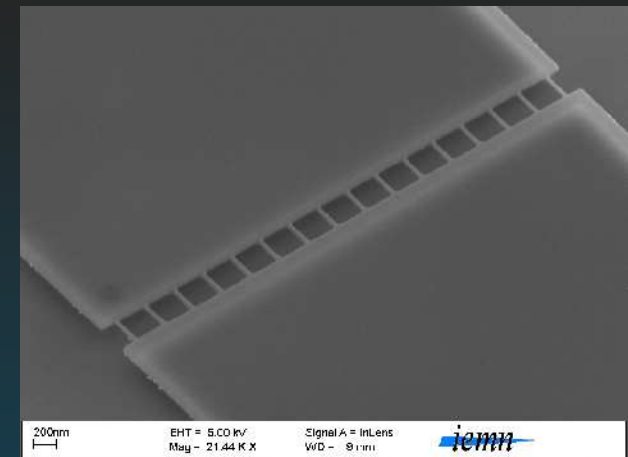
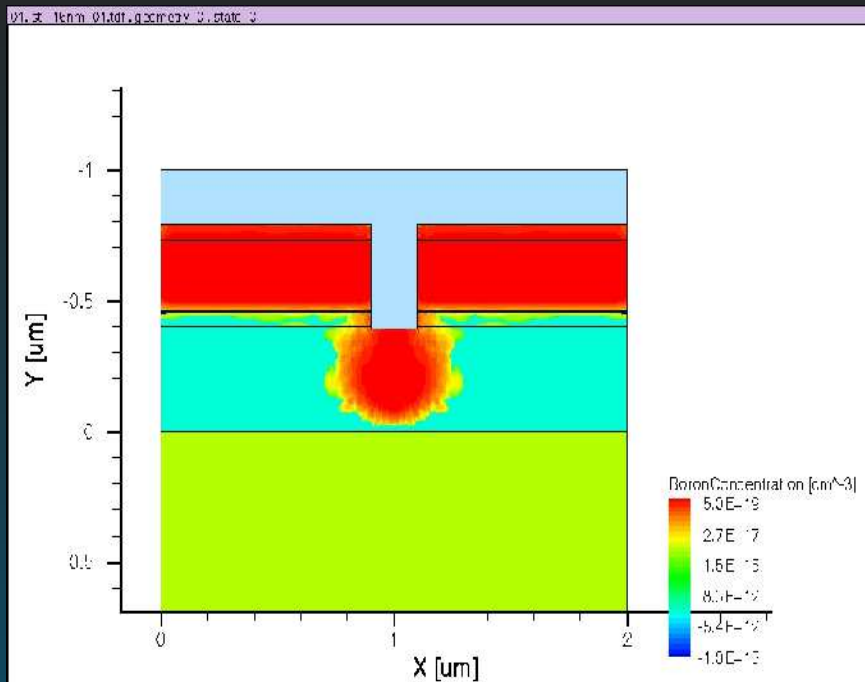


Damage profile



# Implantation Modeling Example

- 2D Implant modeling for nanowire fabrication



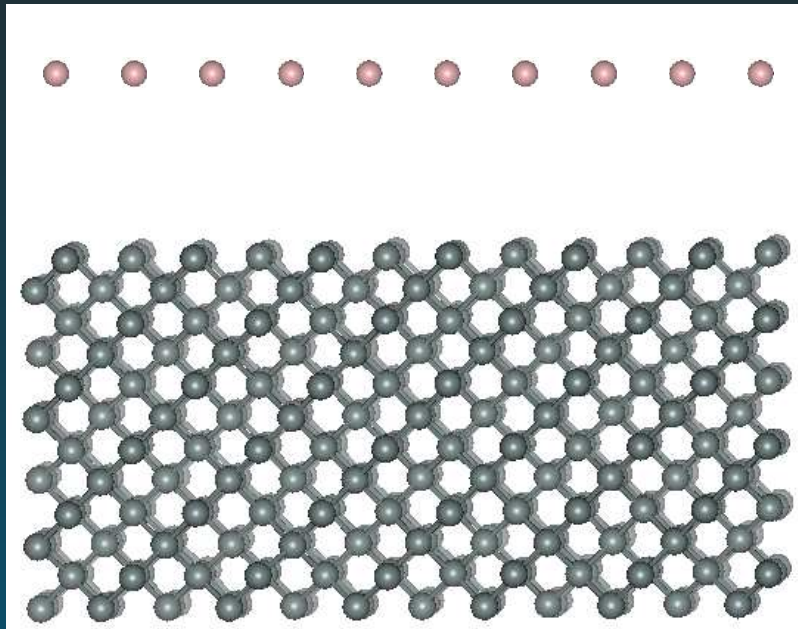
Creation of Silicon nanowire by anisotropic etching with a damage gradient  
Optimisation (Dopant, Dose, Energy) with simulation

*Vikram Passi et al., UCL, NANOSIL WP 2.1 (unpublished results)*

### Standard Technology

Ionic implantation for the dopant with various energy & dose

Boron atoms



After implantation:

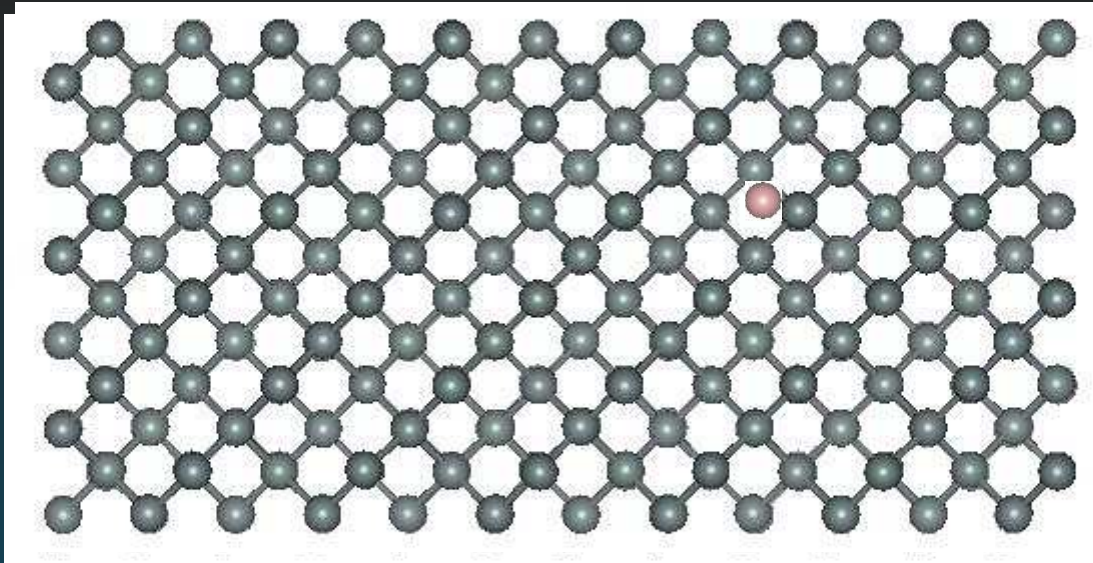
- Dopants in an interstitial position electrically inactive
- Defects created : interstitials, vacancies, aggregate, amorphous pocket

→ Annealing step mandatory

# Diffusion Modeling (2)

## Boron Kick-out

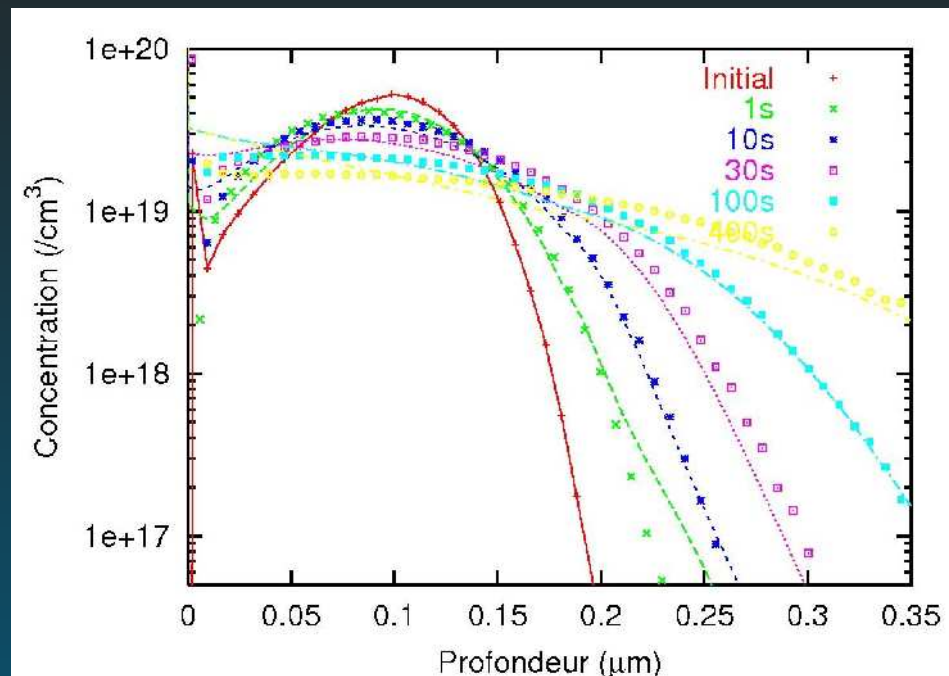
What's going on during annealing? Example for boron



- Interstitial Boron mobile form
- Immobile Boron impurity (electrically active) and creation of Si interstitial
- Diffusion and recombinaison of Si interstitial.
- Kick-out of a boron atoms by an another Si interstitial
- ...
- The junction depth and the activated dose results from the contribution of all these mechanisms
- Standard process simulator used Fick law and diffusion- reaction equations to describe the the intreaction with point defects and mechanism like kick-out

# Diffusion Modeling (3)

- Application: Evolution of doping profile during annealing critical for electrical properties (see also slide 44)



Example of Boron diffusion profile diffusion

# Oxidation and stress modeling (1)

JOURNAL OF APPLIED PHYSICS

VOLUME 36, NUMBER 12

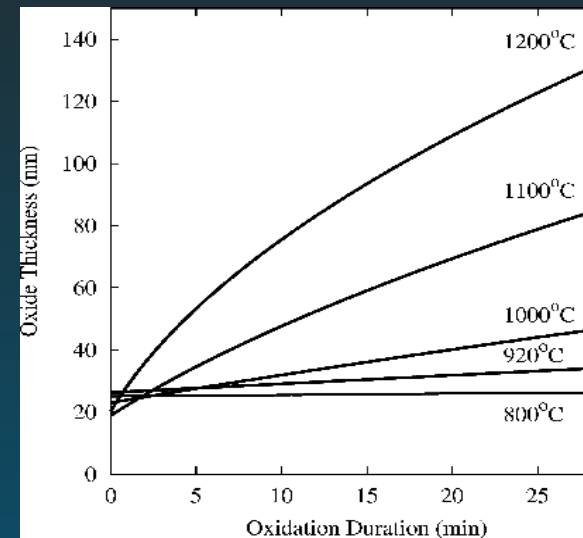
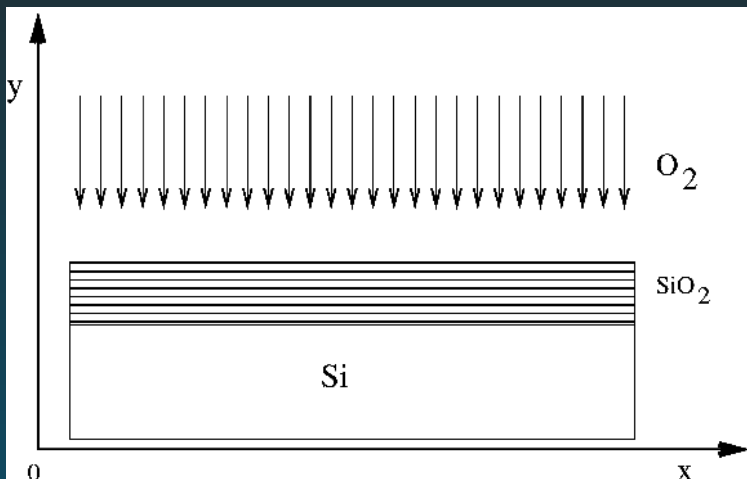
DECEMBER 1965

## General Relationship for the Thermal Oxidation of Silicon

B. E. DEAL AND A. S. GROVE

*Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation,  
Palo Alto, California*

(Received 10 May 1965; in final form 9 September 1965)

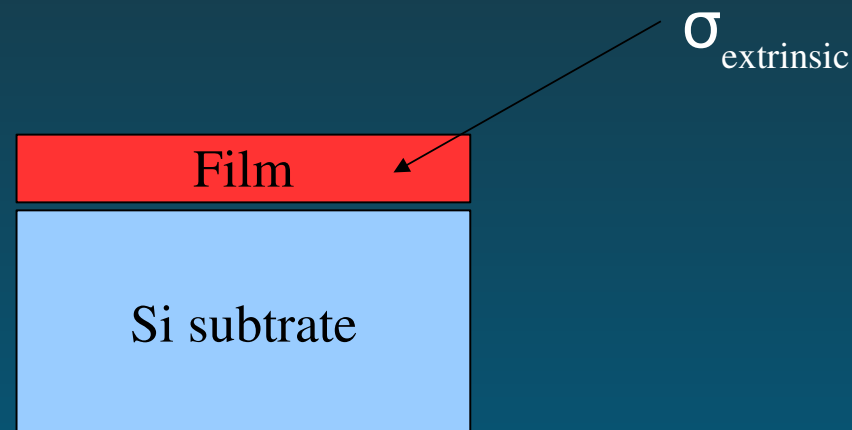


Process simulator : generalised Deal& Grove oxidation model ( diffusivity & and reaction rate stress-dependent) to take into account the stress (volume expansion)

# Various source of stress

| Stress sources             | Technical Process  |
|----------------------------|--|
| Thermal Stress             | Thermal variation during various processing step           |
| Topological induced Stress | Thermal growth (oxidation, silicidation), etching          |
| Intrinsic Stress           | Film deposition process (nitride, polysilicon, metals....) |
| Extrinsic stress           | Structural modifications of films                          |
| High doping induced stress | Steep doping gradients                                     |

Example : modeling of stress generated by deposition of thin film  
introduction of an extrinsic stress and mechanical equilibration



# Example: Oxidation and stress modeling

JOURNAL OF APPLIED PHYSICS

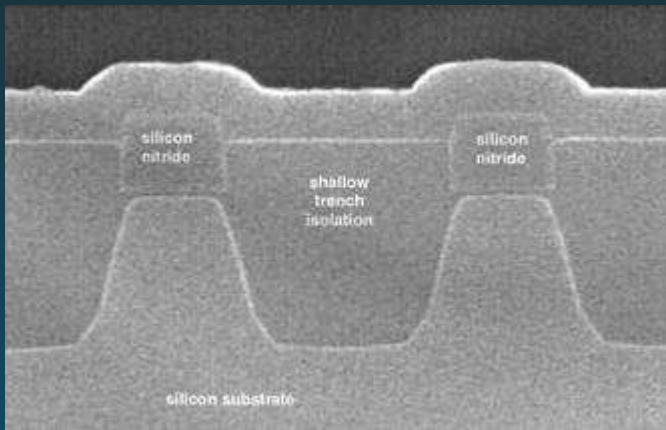
VOLUME 94, NUMBER 9

1 NOVEMBER 2003

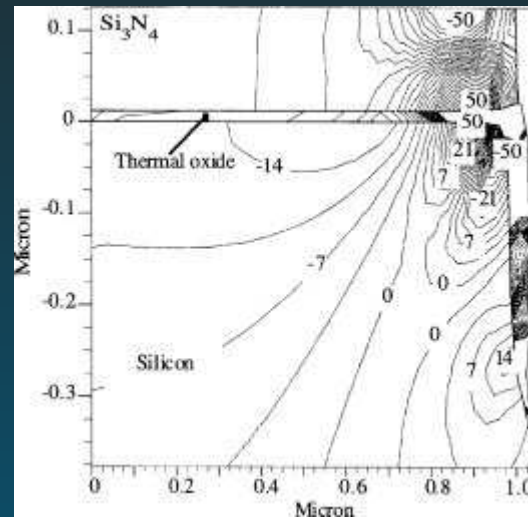
## Strain determination in silicon microstructures by combined convergent beam electron diffraction, process simulation, and micro-Raman spectroscopy

Vincent Senez<sup>a)</sup>

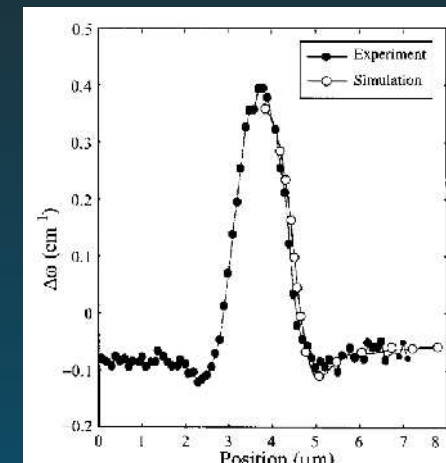
*IEMN-ISEN, UMR CNRS-8520, Avenue Poincaré, B.P. 69, 59652 Villeneuve d'Ascq cédex, France*



STI (Shallow stress Isolation structure)



Stress field (TCAD)



μRS (experiment vs simulation)

but for Large structure

# Conclusion

- These different examples => process modeling promising
- Reality is/was more complex (2002)
  - Example taken from different or academic softwares
  - Difficulty to describe TED Boron, segregation effects, ultra-thin oxidation, silicidation....
  - No real stress modeling capabilities (commercial tool)
- The Mark Law definition: « **TCAD : yesterday's technology modeled tomorrow** »



M. E. Law, IBM J. Res. Dev., Vol. 46, n°2/3, March 2002



# Conclusion

- « *TCAD : yesterday's technology modeled tomorrow* » still true ?
- No:
  - Large progress have been performed in diffusion modeling ( Support by the EC: European project Rapid, Frenotech, PullNaNo,Atomics)
  - Progress have been done for « simple » stress modeling
  - The merging of the major TCAD firms (Avant!, ISE, Synopsys) ~ market 80%  
DIOS (meshing, numerical stability), TAURUS (3D capabilities, Implantation, stress) and TSUPREM-IV (oxidation modeling) to the FLOOPS-ISE (new diffusion modeling)
  - More contribution and more insight with atomistic modeling
  - There is also a part of « dream »: simulation can not replace characterisation
  - Script models speed up the pipeline (M. Law) : University (models)=>TCAD company (software) => Semiconductor Company ? No but more
- Yes:
  - Complexity increase : Stress Engineering (Slide 8), New material (Ge), Laser Annealing & Solid Phase Epitaxy.....

## Recent progress in the modeling of stress

# Modeling SiGe S/D stress field

APPLIED PHYSICS LETTERS 86, 023103 (2005)

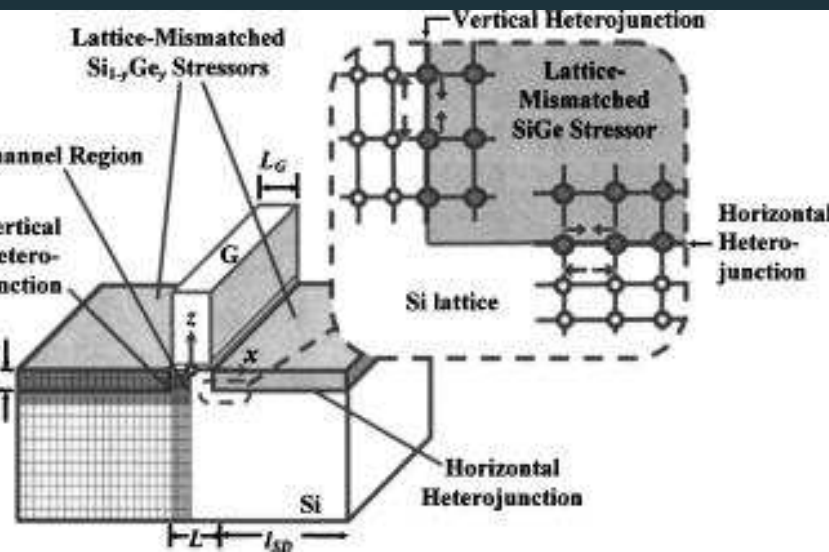
## Finite-element study of strain distribution in transistor with silicon-germanium source and drain regions

Yee-Chia Yeo<sup>a)</sup>

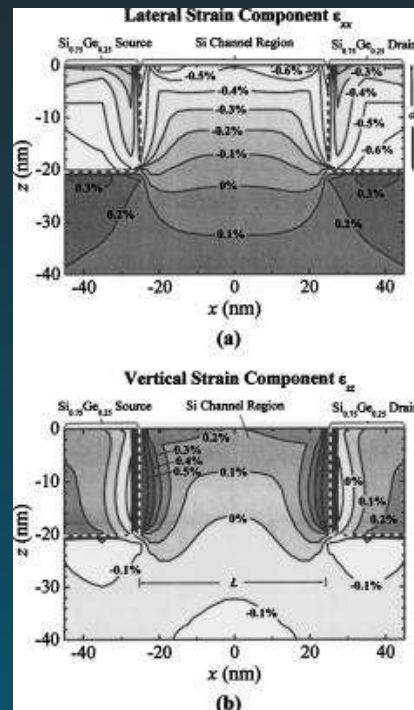
Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, 119260, Singapore

Jisong Sun

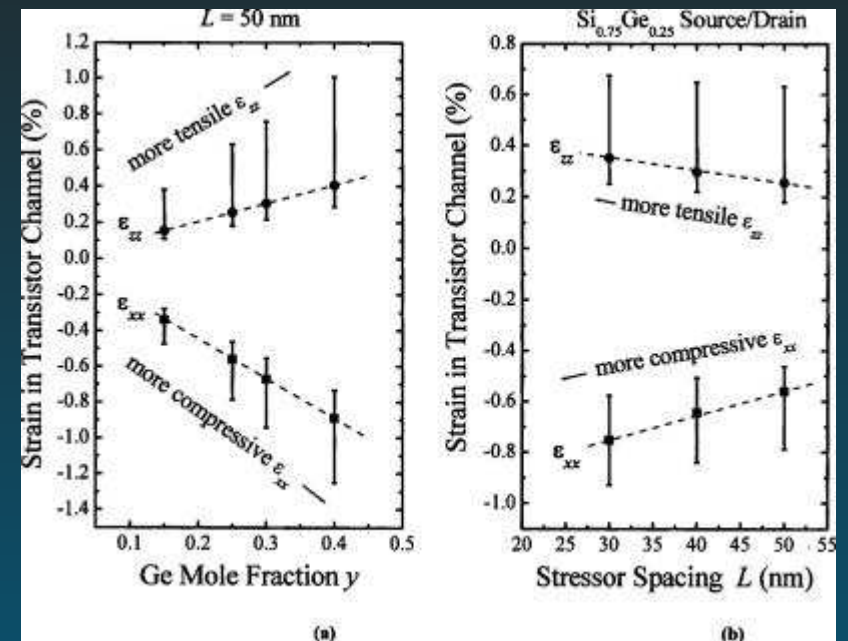
Agency for Science, Technology, and Research, Data Storage Institute, DSI Building, 5, Engineering Drive 1, 117608, Singapore



Principle of Lattice-mismatched stressor



Lateral & Vertical strain induced



Evolution of channel strain as a function of the Ge fraction and the spacer with

Y. Yeo et al., *Appl. Phys. Lett.*, 86, 023103, 2005

# SiGe S/D scalability

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 7, JULY 2006

1897

## Scalability of the $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain Technology for the 45-nm Technology Node and Beyond

Geert Eneman, Peter Verheyen, Rita Rooyackers, Faran Nouri, *Senior Member, IEEE*, Lori Washington, Robert Schreutelkamp, Victor Moroz, Lee Smith, *Member, IEEE*, An De Keersgieter, Malgorzata Jurczak, and Kristin De Meyer, *Senior Member, IEEE*

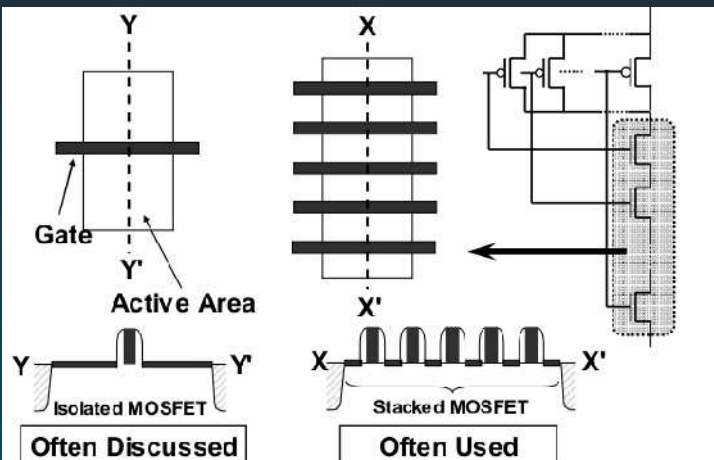
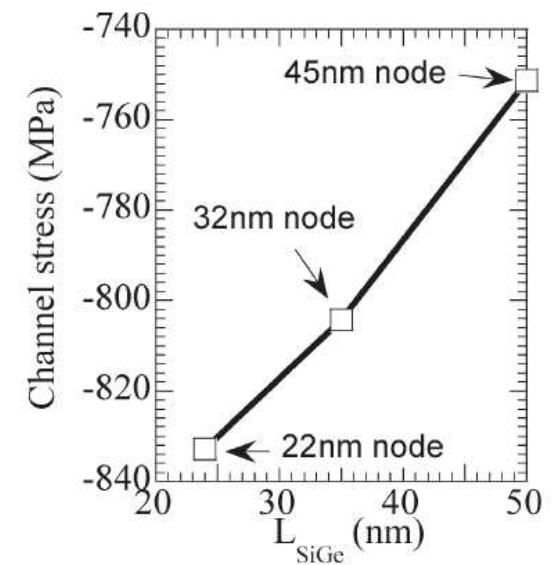
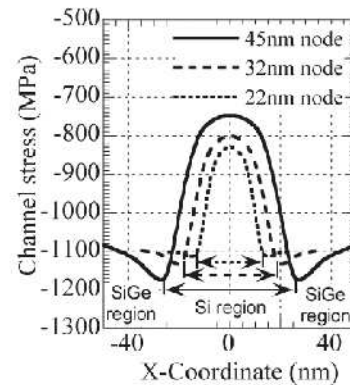


Fig.1 Schematic view of MOSFET layout which is often used and often discussed. Stacked MOSFET which is often used in actual products should be discussed.

TABLE I  
TECHNOLOGY PARAMETERS FOR THE 45-, 32-, AND 22-nm TECHNOLOGY NODE

|           | $L_g$ (nm) | $L_{SD}$ (nm) | $L_{SiGe}$ (nm) | $t_{SiGe}$ (nm) | $W$ (nm) |
|-----------|------------|---------------|-----------------|-----------------|----------|
| 45nm node | 18         | 100           | 50              | 60              | 100      |
| 32nm node | 13         | 70            | 35              | 50              | 70       |
| 22nm node | 9          | 50            | 24              | 45              | 50       |



Mean compressive channel stress does not decrease with downscaling

G. Eneman et al., IEEE Trans. on Electron Device, Vol. 86, 023103, 2005

# Modeling CESL stress

## Multi-Layer Model for Stressor Film Deposition

K.V. Loiko, V. Adams, D. Tekleab, B. Winstead, X.-Z. Bo, P. Grudowski, S. Goktepe, S. Filipiak, B. Goolsby, V. Kolagunta, and M.C. Foisy

Austin Silicon Technology Solutions, Freescale Semiconductor, Inc.  
3501 Ed Bluestein Blvd, Austin, TX 78721  
Email: loiko@freescale.com

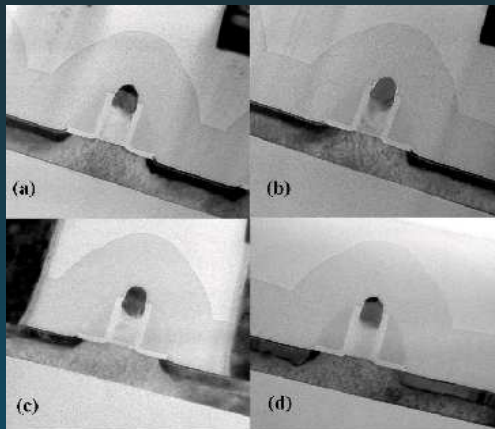


Figure 1. TEMs of 35nm gates with highly stressed ESL films as a function of gate poly pitch: (a) 0.26 μm, (b) 0.38 μm, (c) 0.63 μm, (d) 1.04 μm.

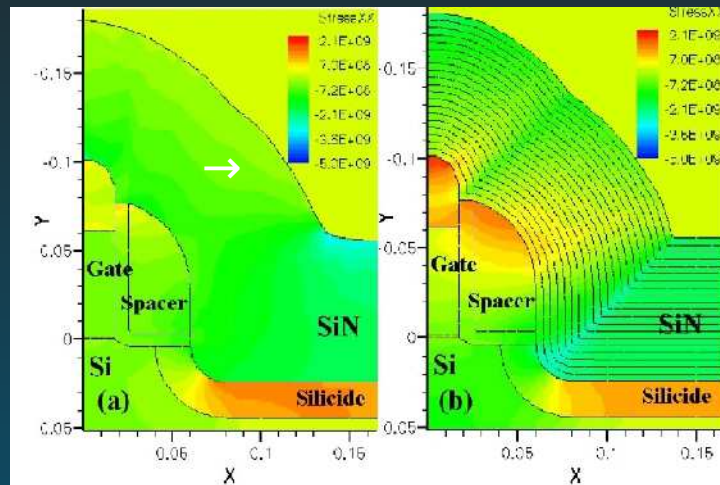


Figure 7. Contours of lateral stress (Pa) in 35nm transistor structures with 20nm source/drain recess simulated using (a) single-layer and (b) 20-layer deposition of nitride with compressive intrinsic stress.

Large difference between mono and multi step deposition

K. V. Loiko et al., SISPAD 2006

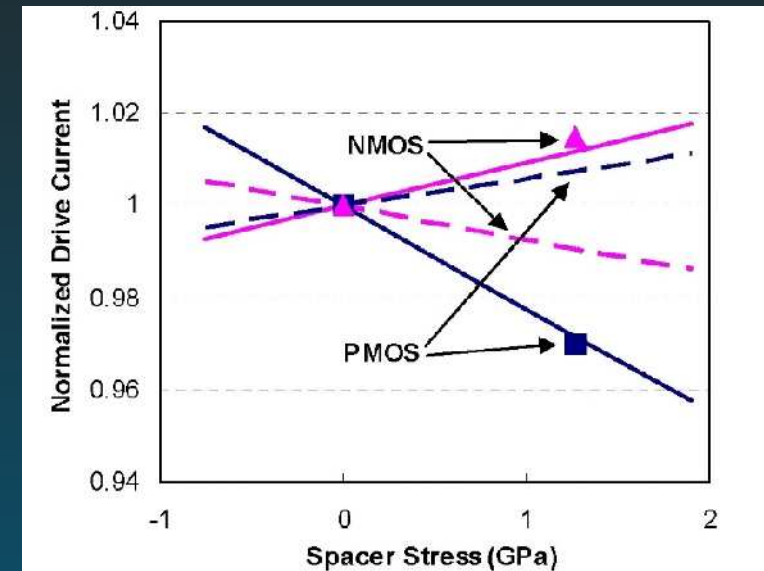


Figure 8. Experimental data (symbols), multi-layer (solid lines) and single-layer (dashed lines) simulation results on NMOS (lensile ESL) and PMOS (compressive ESL) drive current vs. spacer stress.

Opposite experimental trends with mono step deposition !

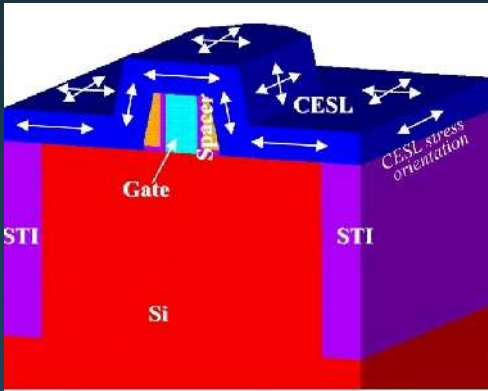
# Engineering the CESL stress

814

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 4, APRIL 2007

## Method for Managing the Stress Due to the Strained Nitride Capping Layer in MOS Transistors

Stéphane Orain, Vincent Fiori, Davy Villanueva, Alexandre Dray, and Claude Ortolland



3D Ansys Simulation

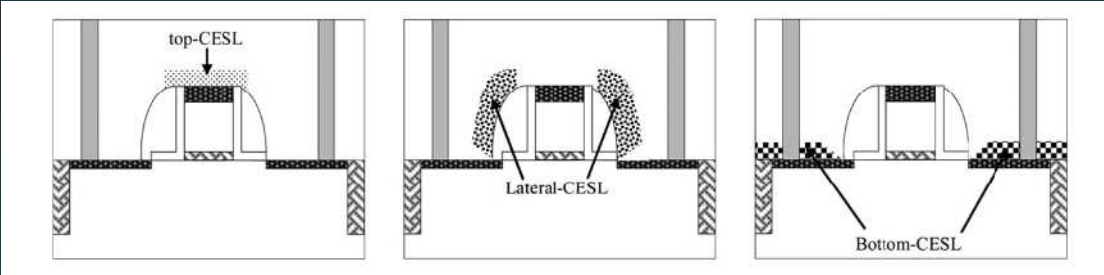


TABLE I  
SUMMING UP THE IMPACT OF ALL THE CESL EFFECTS (C = CORNER, D = DIRECT, AND I = INDIRECT) FOR EACH CESL ZONE (TOP, LAT. = LATERAL, AND BOT. = BOTTOM)

|       |    | Corner         | Top                            | Lat.                           | Bot.           |
|-------|----|----------------|--------------------------------|--------------------------------|----------------|
| Long  | Sx | C <sup>+</sup> | D <sup>-</sup>                 | 0                              | D <sup>+</sup> |
|       | Sy | C <sup>+</sup> | D <sup>-</sup>                 | 0                              | D <sup>+</sup> |
|       | Sz | 0              | I <sup>-</sup> /D <sup>-</sup> | 0                              | 0              |
| Short | Sx | C <sup>+</sup> | 0                              | D <sup>-</sup>                 | D <sup>+</sup> |
|       | Sy | C <sup>+</sup> | 0                              | D <sup>-</sup>                 | D <sup>+</sup> |
|       | Sz | 0              | I <sup>-</sup>                 | I <sup>-</sup> /D <sup>-</sup> | D <sup>-</sup> |

LEGEND:  
 C : Corner effects  
 D : Direct effects  
 I : Indirect effects  
 - : Compressive stress  
 + : tensile  
 0 : no or low impact

Which part of the CESL influence the channel stress ?

- Complex answer (Long<=>short device) !
- Such table provide guidelines for device optimisation
- Geometry of the spacer (L or D shape) important

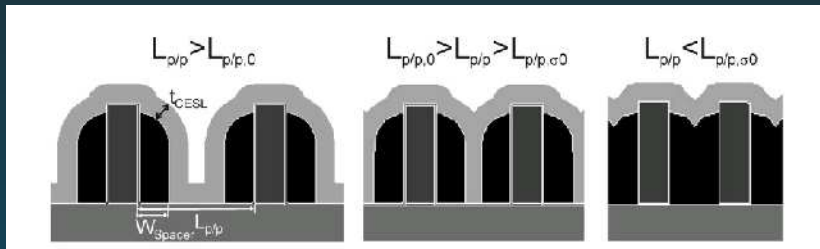
# Scalability of CESL

1446

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 6, JUNE 2007

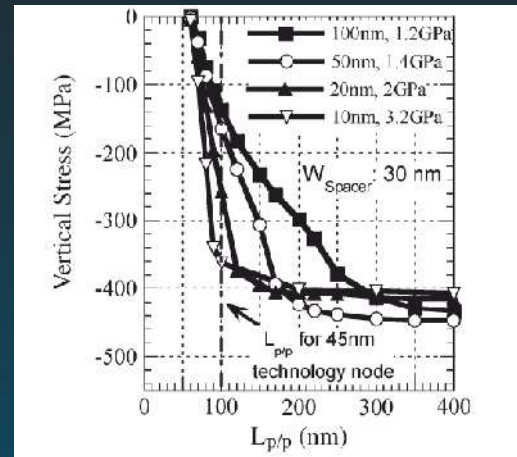
## Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study

Geert Eneman, Peter Verheyen, An De Keersgieter, Malgorzata Jurczak, and Kristin De Meyer, *Senior Member, IEEE*

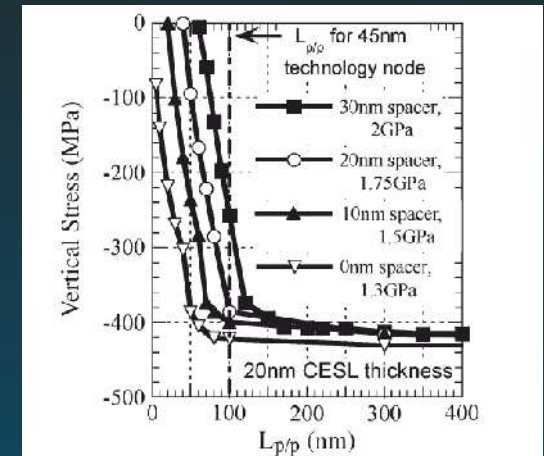


Poly to Poly Distance:  $L_{p/p}$

$$L_{p/p} > L_{p/p,0} = 2 \cdot t_{CESL} + 2 \cdot W_{Spacer}$$



For large CESL thickness, decreasing  $L_{p/p}$  leads to stress reduction

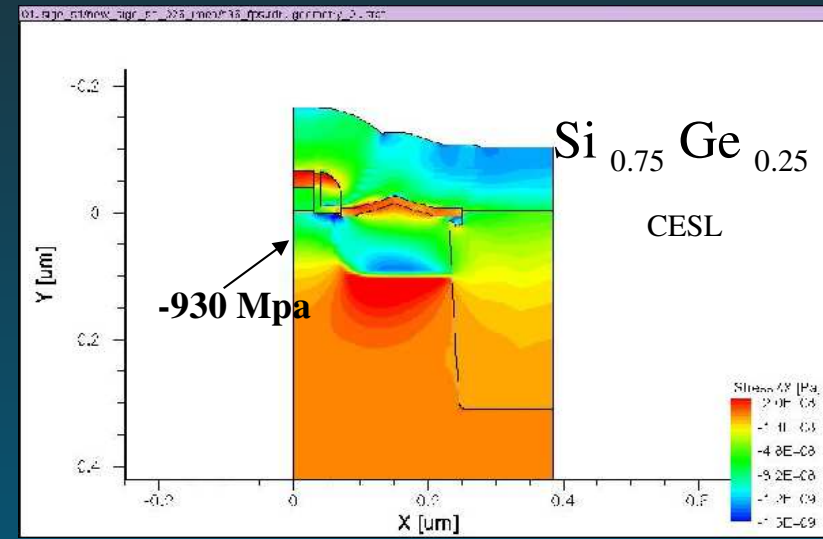
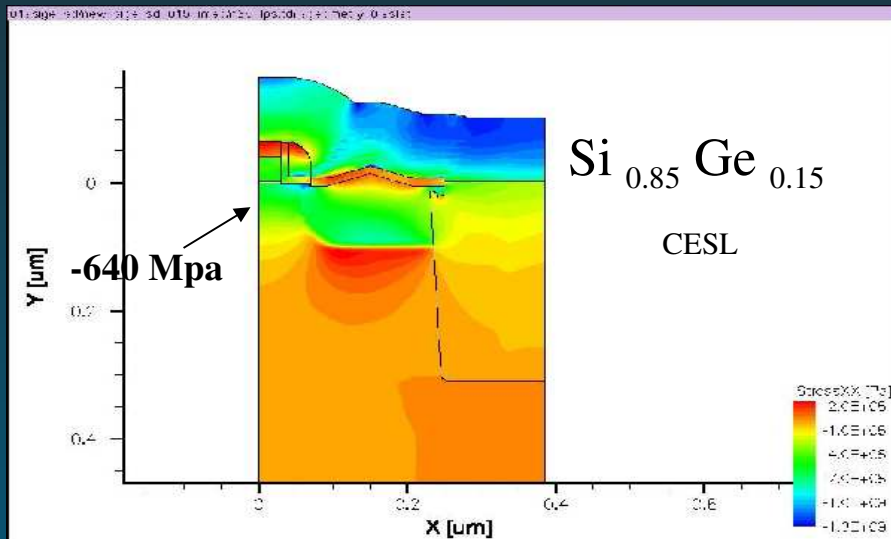
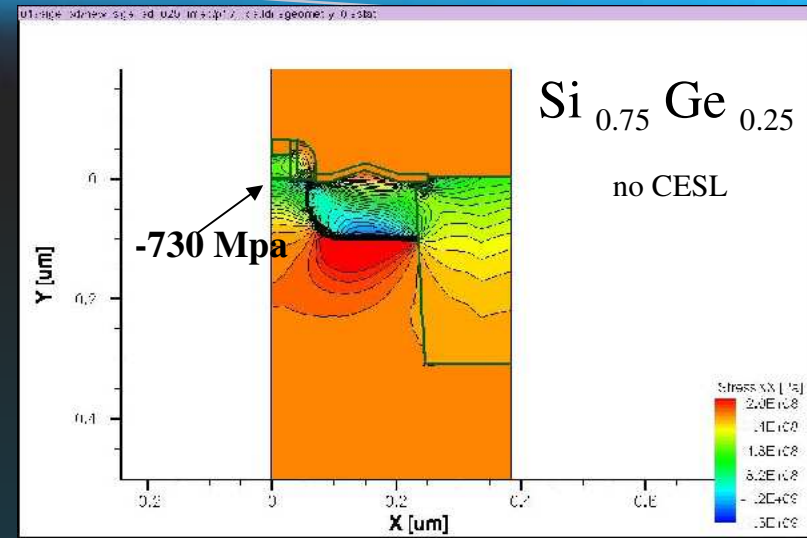
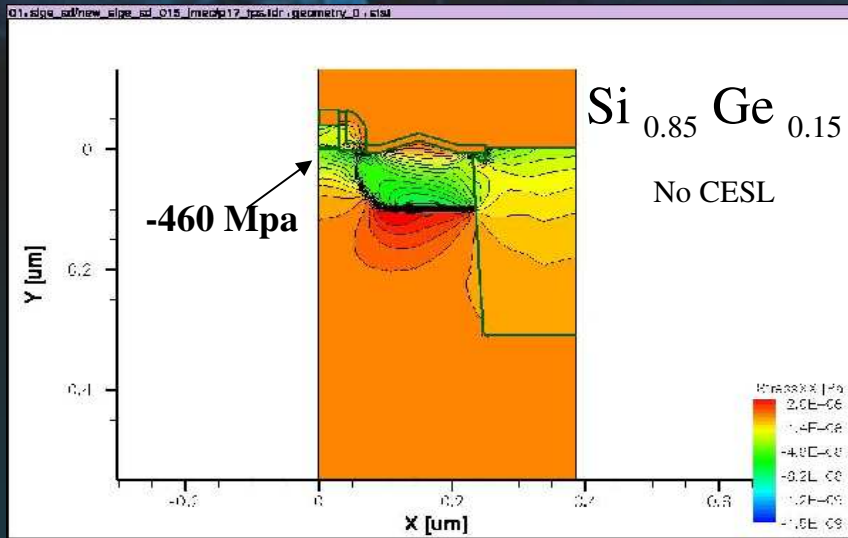


Influence of spacer width on vertical stress for decreasing  $L_{p/p}$

↘ CESL thickness is no sufficient, spacer dimensions must be scaled

G. Eneman et al., *IEEE Trans. on Electron Device*, Vol. 54, N°6, June, 2007

# S/D SiGe & CESL modeling with SProcess



C. Krzeminski, PULLNANO Results (unpublished)



# Conclusion

- Large progress have been performed in the stress modeling with the support of experimental development, study of topography influence, evaluation of scalability (SiGe S/D or Stress Liner)
- There was one issue :

| Journal or major proceedings conferences Publications (2001-2008) | Number | Proprietary simulator | “Old” simulator Taurus/ Tsuprem-IV | Mechanical simulator (Ansys/ FEMLAB) | Sentaurus Process |
|---|--------|-----------------------|------------------------------------|--------------------------------------|-------------------|
| TCAD&stress   | 14     | 30%                   | 40%                                | 30%                                  | 0%                |

- But large progress have been performed recently in the last version of Sentaurus Process as shown by the last PullNANO Results
- Still a lot of work: Stress Memorization, SiC stressor.....

## Progress in diffusion modeling

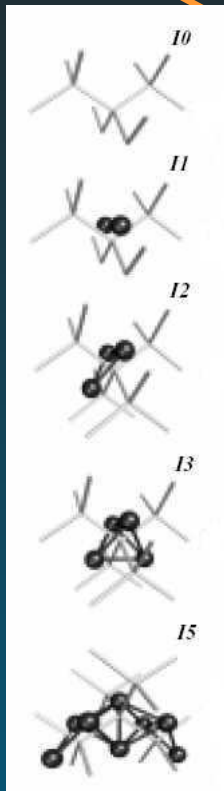
# Extended defects

Role on extended defects formed after ion implantation of dopants

2 atoms

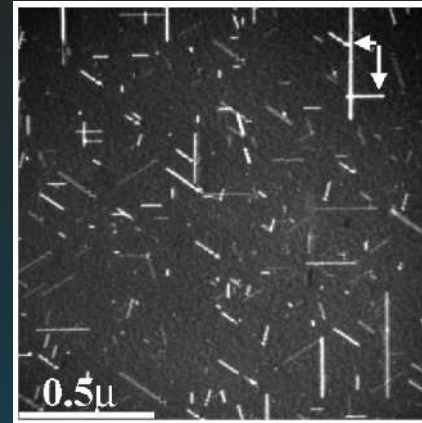
Small clusters

Bongiorno, Europhys. Lett. 50, 608 (2000).



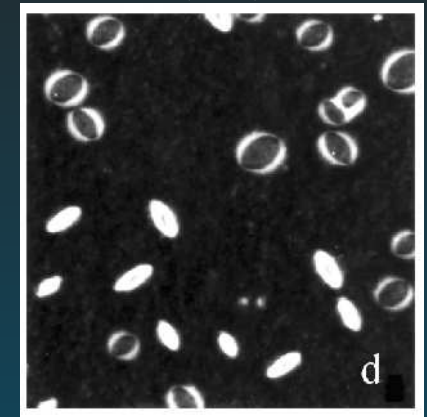
{113} defects

Cherkashin, MRS Symp. Proc. 810, C3.7 (2004).

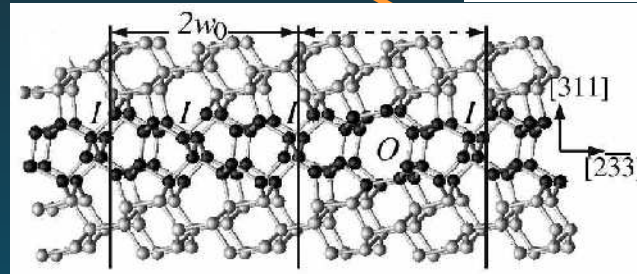


CEMES/LAAS

Claverie, MRS Symp. Proc. 610, B11.6 (2000).

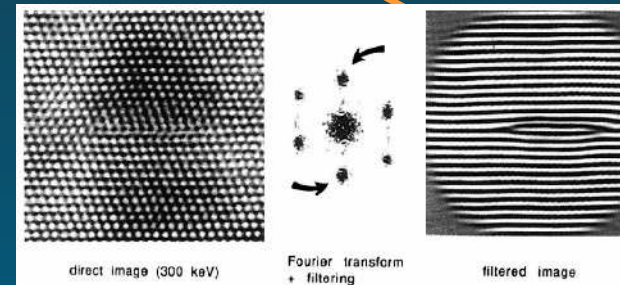


Dislocation loops



Kim, Phys. Rev. Lett. 84, 503 (2000).

Claverie, Mat. Sc. Semicond. Proc. 3, 269 (2000).

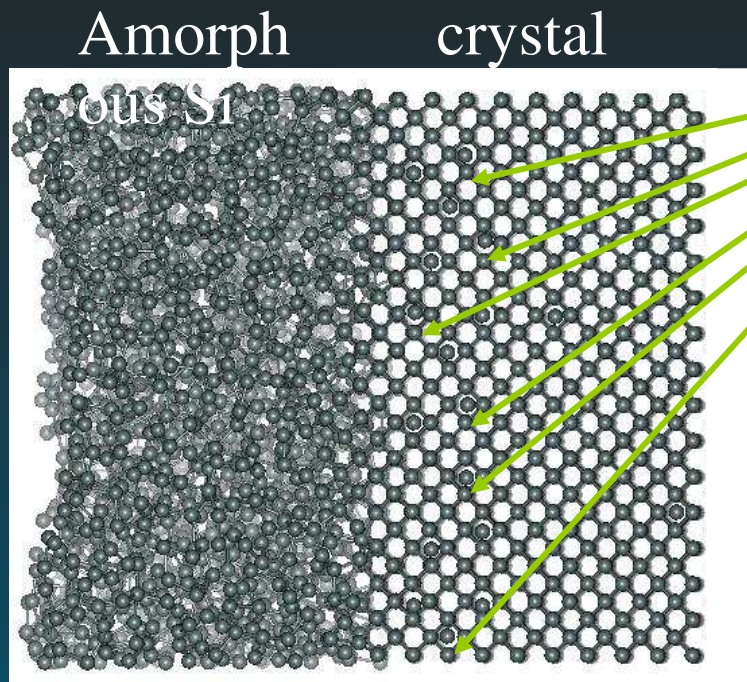


~ 10000 atoms

# Boron Transient enhanced diffusion (TED) & extended defects

→ Common origin : the supersaturation of interstitials formed by the implantation step

Ex in the case of a preamorphisation :



Excess or supersaturation of interstitials just behind the amorphous /cristalline interface

During annealing :

Precipitation into extended defects

Accelerated diffusion of boron

→ Need to couple a model of extended defects to conventionnal packages of dopant diffusion

# nucleation, pure growth and Ostwald ripening of defects

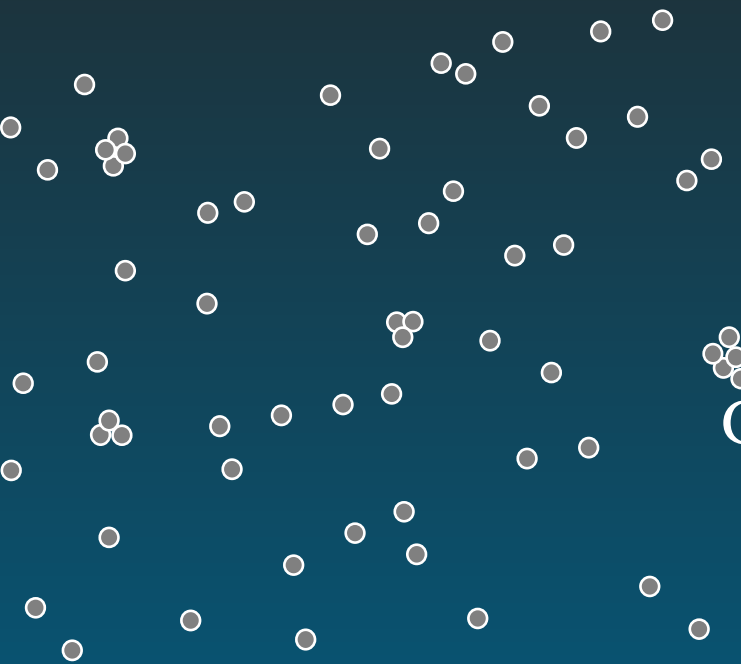
- Nucleation of extended defects – reduction of the system energy



# nucleation, pure growth and Ostwald ripening of defects

- Nucleation of extended defects – reduction of the system energy
- Growth of the nuclei by absorption of the residual interstitials

→ pure growth

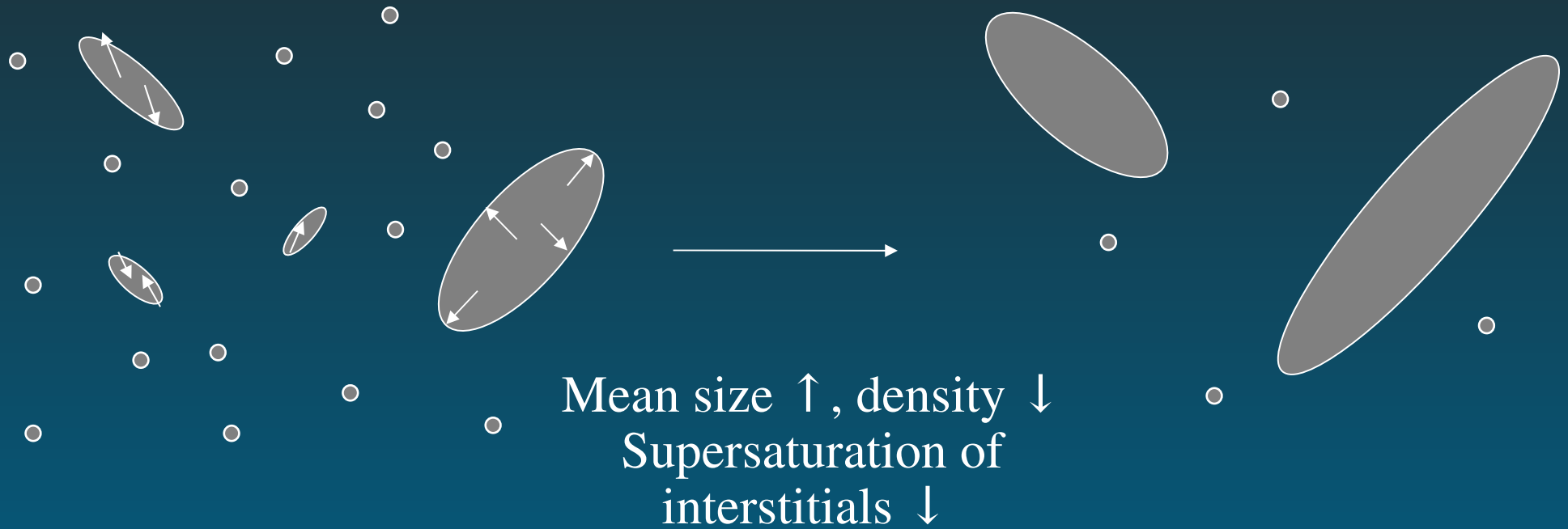


Growth of the existing defects  
Supersaturation ↓



# Nucleation, pure growth and Ostwald ripening of defects

- Nucleation of extended defects – reduction of the system energy
- Growth of the nuclei by absorption of the residual interstitials  
→ pure growth
- Ostwald ripening (dynamical equilibrium) extended defects  $\leftrightarrow$  interstitial supersaturation



# TED and Dislocation Loops (DL)

JOURNAL OF APPLIED PHYSICS

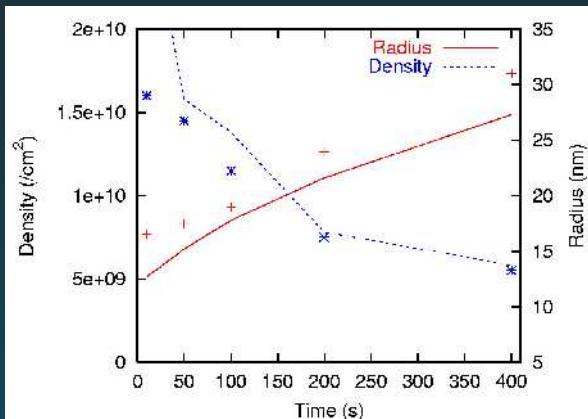
VOLUME 85, NUMBER 12

15 JUNE 1999

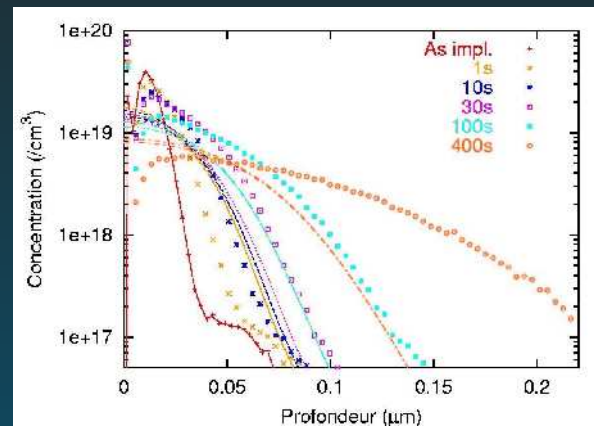
## Modeling of the transient enhanced diffusion of boron implanted into preamorphized silicon

E. Lampin<sup>a)</sup> and V. Senez  
*IEMN-Dpt. ISEN, UMR CNRS 9929, BP 69, 59652 Villeneuve d'Ascq Cédex, France*

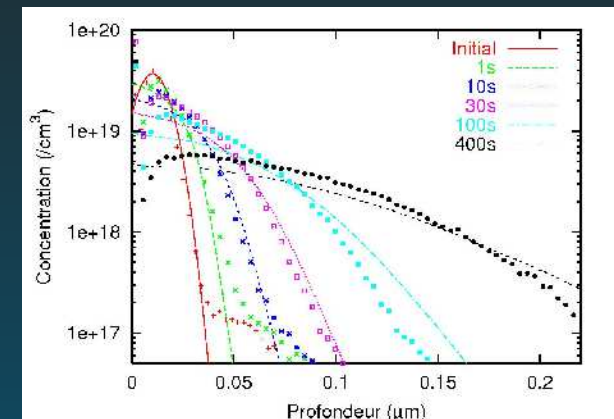
A. Claverie  
*CEMES-CNRS, BP 4347, 31055 Toulouse Cédex, France*



Evolution of density and size of Dislocations loops (DL)



Final TED diffusion effects underestimated if DL not considered



Good predictivity of TED effects with the incorporation of DL and Si interstitials evolution



# Atom-by-atom model of defects evolution

Appl. Phys. A 76, 1025–1033 (2003)  
DOI: 10.1007/s00339-002-1944-0

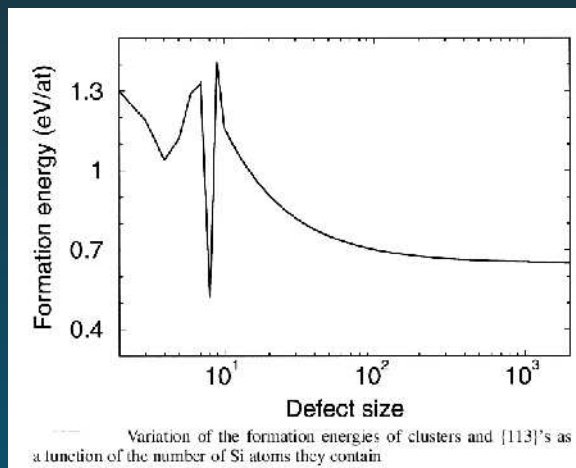
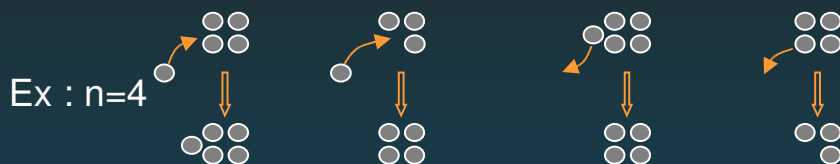
Applied Physics A  
Materials Science & Processing

A. CLAVERIE<sup>1, (cor)</sup>  
B. COLOMBEAU<sup>1</sup>  
B. DE MAUDUIT<sup>1</sup>  
C. BONAFOS<sup>1</sup>  
X. HEBRAS<sup>1,2</sup>  
G. BEN ASSAYAG<sup>1</sup>  
F. CRISTIANO<sup>2</sup>

## Extended defects in shallow implants

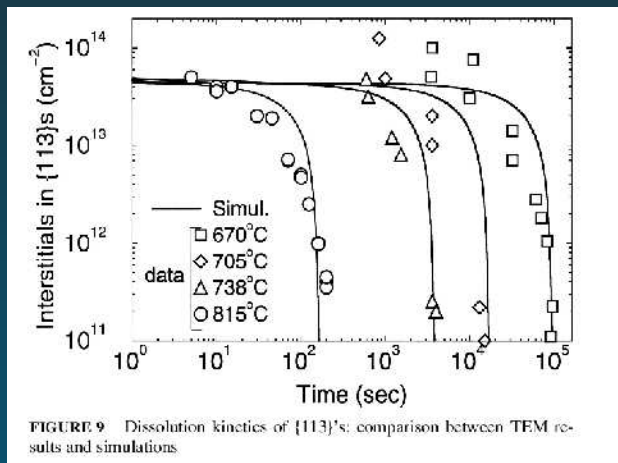
<sup>1</sup> Ion Implantation Group CNRS Toulouse, CEMES/CNRS, BP 4347, 31055 Toulouse Cedex, France  
<sup>2</sup> Ion Implantation Group CNRS Toulouse, LAAS/CNRS, 7 Ave. Colonel Roche, 31055 Toulouse Cedex, France

$$\frac{dN_n}{dt} = -[F_n N_n - F_{n-1} N_{n-1}] + R_{n+1} N_{n+1} - R_n N_n$$

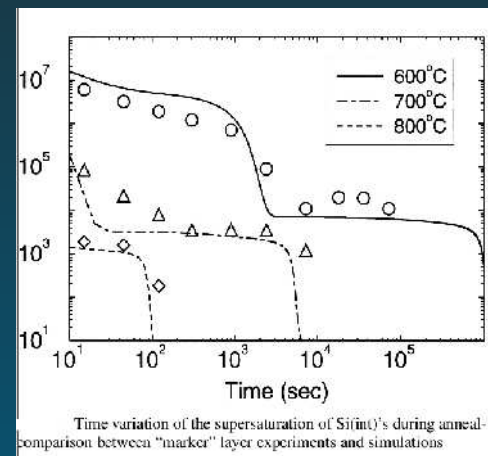


Formation energies for clusters, {113} Cowern et al.

A. Claverie et al., Appl. Phys. A, Vol. 76, 2003 (Frendtech results)



Dissolution of {113}'s



Evolution of Si interstitials as a function of the time

# Coupling atom-by-atom model & diffusion

JOURNAL OF APPLIED PHYSICS

VOLUME 94, NUMBER 12

15 DECEMBER 2003

## Prediction of boron transient enhanced diffusion through the atom-by-atom modeling of extended defects

E. Lampin<sup>a)</sup>

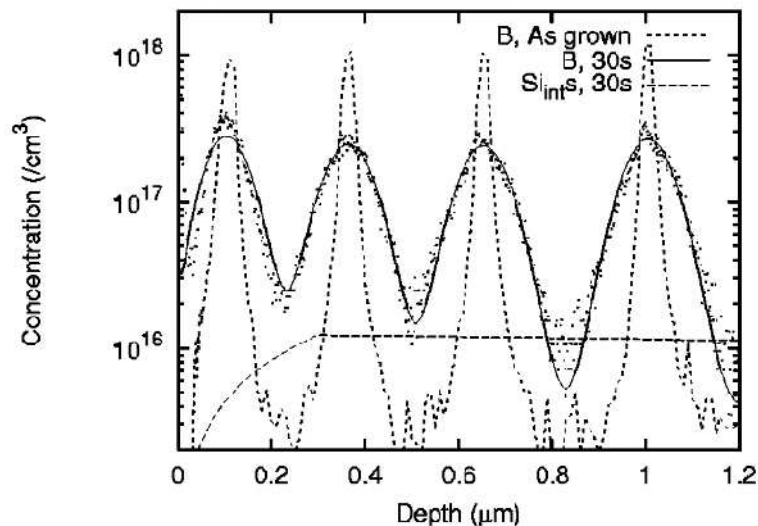
*IEMN/ISEN, UMR CNRS 8520, 59652 Villeneuve d'Ascq, Cedex, France*

F. Cristiano, Y. Lamrani, and A. Claverie

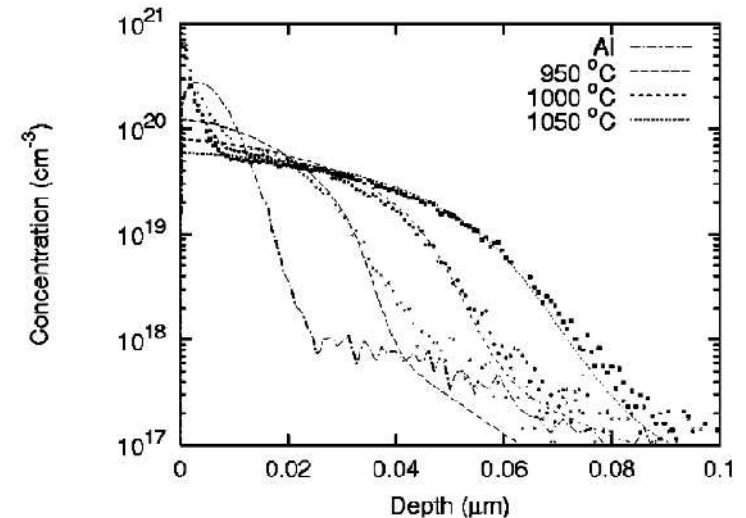
*Ion Implantation Group, CEMES/IAAS-CNRS, 31055 Toulouse, France*

B. Colombeau and N. E. B. Cowern

*Advanced Technology Institute, University of Surrey, Guildford, GU2 7XH Surrey, United Kingdom*



Nice simulation of TED effects for marked layers experiments



Nice simulation of TED for ultra-low Energy B+ implant

However, simplified model for Sprocess needed

*E. Lampin et al., J. App. Phys., Vol 94, n°12, 2003 (Frendtech results)*

# Advanced annealing schemes

## On a Computationally Efficient Approach to Boron-Interstitial Clustering

Johann Schermer and Peter Pichler  
Fraunhofer-Institute of Integrated Systems and  
Device Technology, Erlangen, Germany

Christoph Zechner  
Synopsys Switzerland LLC  
Zurich, Switzerland

Wilfried Lerch and Silke Paul  
Mattson Thermal Products GmbH  
Dornstadt, Germany

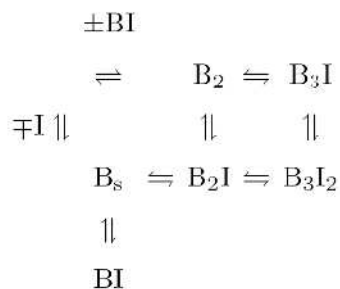


Figure 1: Scheme of reactions for the BICs model

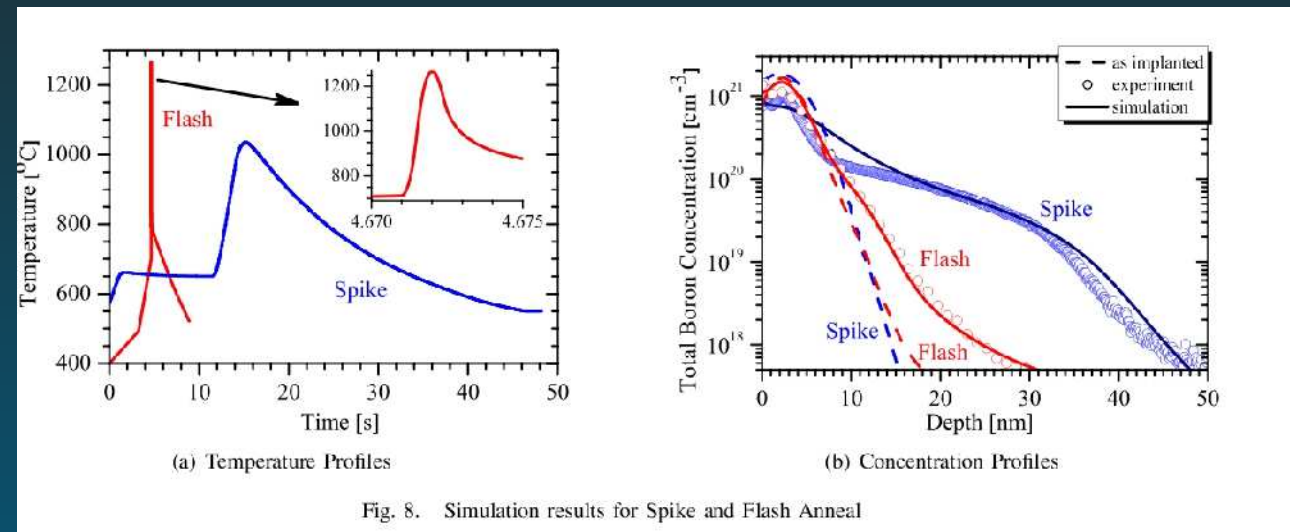
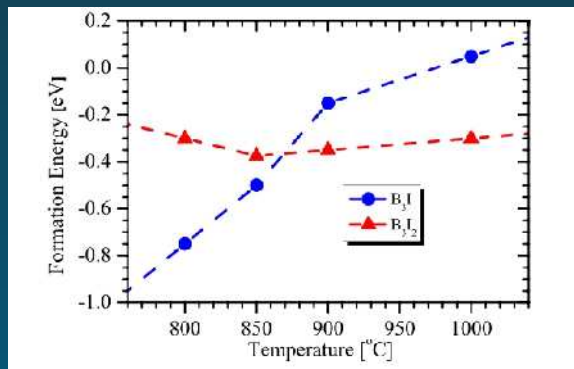


Fig. 8. Simulation results for Spike and Flash Anneal

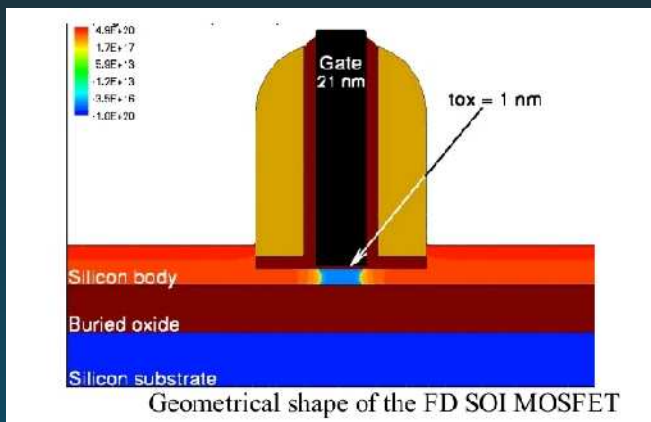
J. Schermer et al., ESSDERC 2007 (PULLNANO results)

# Boron diffusion modeling & Device simulation

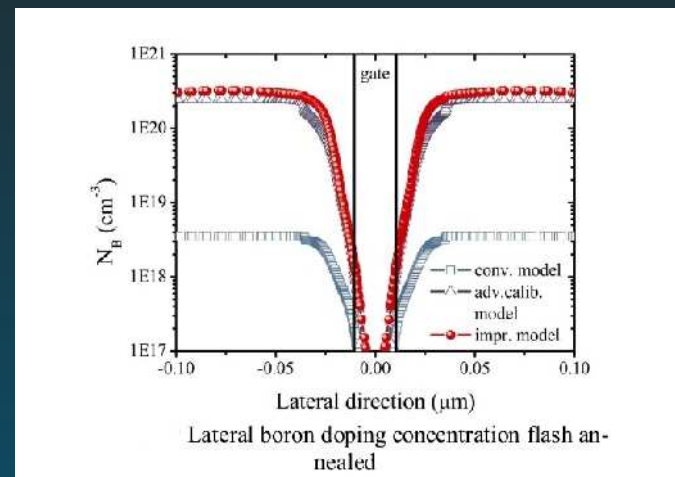
## Process Models for Advanced Annealing Schemes and their Use in Device Simulation

P. Pichler<sup>1,2,\*</sup>, A. Martinez-Limia<sup>1</sup>, C. Kampen<sup>1</sup>, A. Burenkov<sup>1</sup>, J. Schermer<sup>1</sup>, S. Paul<sup>3</sup>, W. Lerch<sup>3</sup>,  
J. Gelpy<sup>4</sup>, S. McCoy<sup>4</sup>, H. Kheyrandish<sup>5</sup>, A. Pakfar<sup>6</sup>, C. Tavernier<sup>6</sup>, D. Bolze<sup>7</sup>

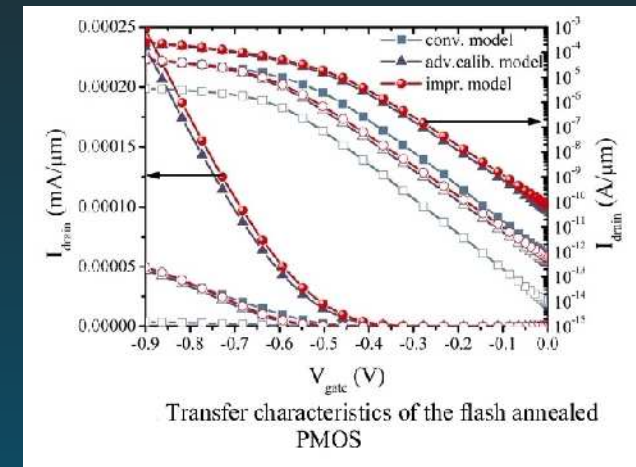
<sup>1</sup>Fraunhofer-Institute of Integrated Systems and Device Technology (IISB),  
Schottkystrasse 10, 91058 Erlangen, Germany



FD nanometric SOI device



Impact of the diffusion modeling on the boron profile

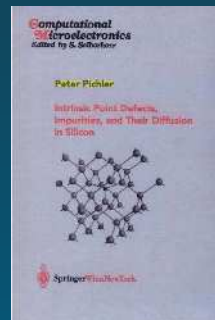


Large impact on the PMOS electrical characteristic predicted

P. Pichler et al., International Workshop on Junction Technology (2008), ATOMICS & PULLNANO Results

# Conclusion

- Large progress have been done in junction processing modeling in the framework of several european projects (Rapid, Frenotech, Pullnano, Atomics) with the collaboration of Synopsys (Zurich)
- Some of the models presented (simplified form) in Sentaurus Process or script transfered to semiconductor compagnies
- But still a lot of work:
  - Influence of stress effects
  - New Material (SiGe S/D, Ge.....)
  - Advanced annealing scheme (laser annealing, solid phase epitaxy)
- More information :



# Part V (prospective)

Atomistic TCAD : towards some computer experiment ?

# Complexity & Limits of a full experimental optimisation (1) ?

- Complex integration in nanodevices

APPLIED PHYSICS LETTERS 90, 241912 (2007)

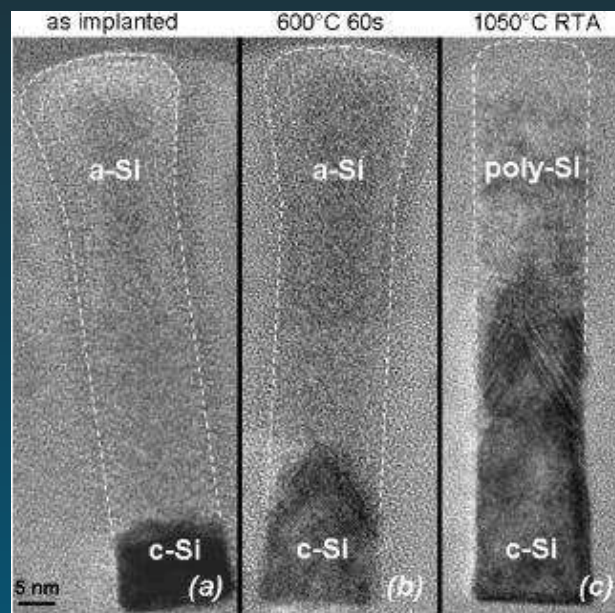
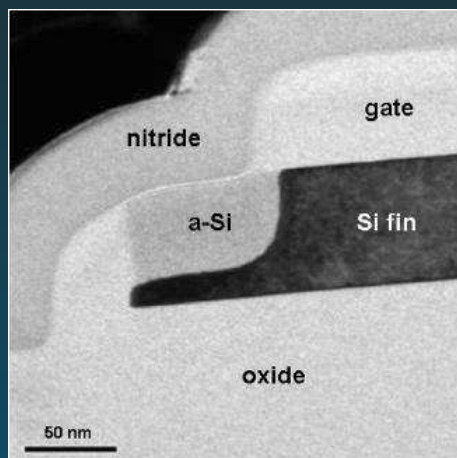
## Solid phase epitaxy versus random nucleation and growth in sub-20 nm wide fin field-effect transistors

R. Dufty,<sup>a)</sup> M. J. H. Van Dal, and B. J. Pawlak  
*NXP Semiconductors, Kapeldreef 75, 3001 Leuven, Belgium*

M. Kaiser and R. G. R. Weemaes  
*Philips Research Laboratories Eindhoven, High Tech Campus 11, 5656 AE Eindhoven, The Netherlands*

B. Degroote, E. Kunnen, and E. Altamirano  
*IMEC, Kapeldreef 75, 3001 Leuven, Belgium*

(Received 26 March 2007; accepted 22 May 2007; published online 13 June 2007)



(PULLNANO results)

# Complexity & Limits of a full experimental optimisation (2) ?

How to characterised diffusion mechanism during a solid phase epitaxy when Time/Temperature window available reduced by recrystallisation ?

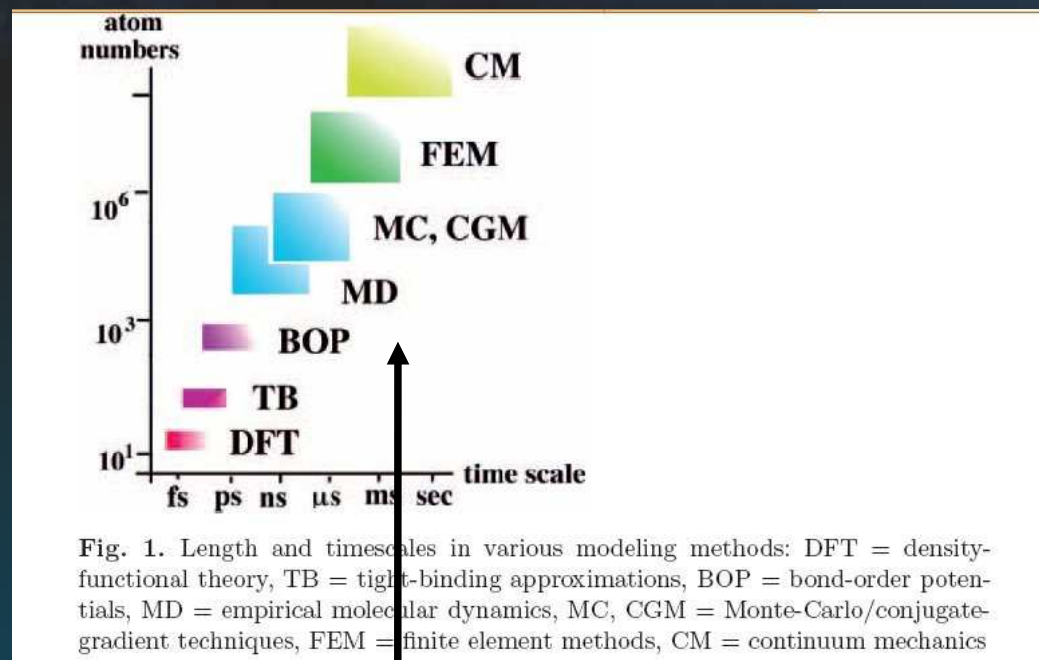


→ A solution proposed by Venezia et al.: Diffusion in completely amorphised silicon layer (but the influence of recrystallisation is not taken into account)

→ Computer experiment (Atomistic TCAD) needed but it will not replace standard TCAD !



# Which method for computer experiment ?



[Scheerschmidt07] [http://www.mpi-halle.de/mpi/publi/pdf/6735\\_06.pdf](http://www.mpi-halle.de/mpi/publi/pdf/6735_06.pdf)

Development of atomistic approach based on molecular dynamics (MD)

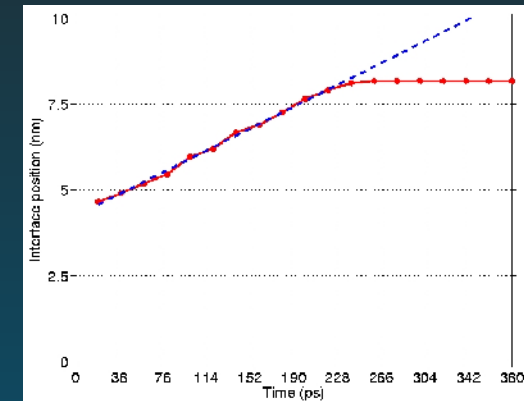
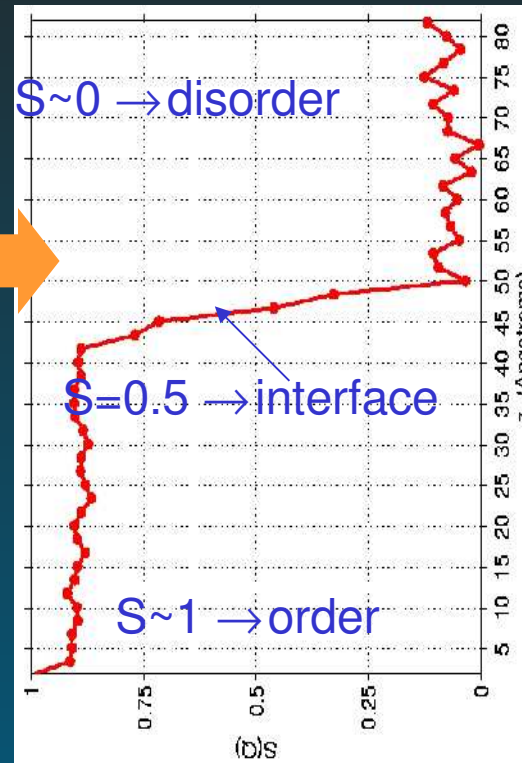
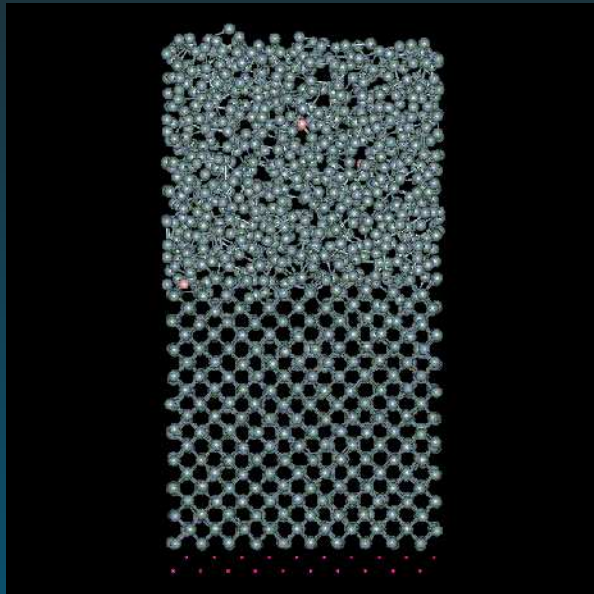
# Molecular Dynamics of LPE, SPE regrowth

Simulation of the annealing and exploitation

Example of annealing, Stillinger-Weber, 1200 K

Extraction interface from 1D structure factor

Procedure repeated to extract the recrystallization velocity

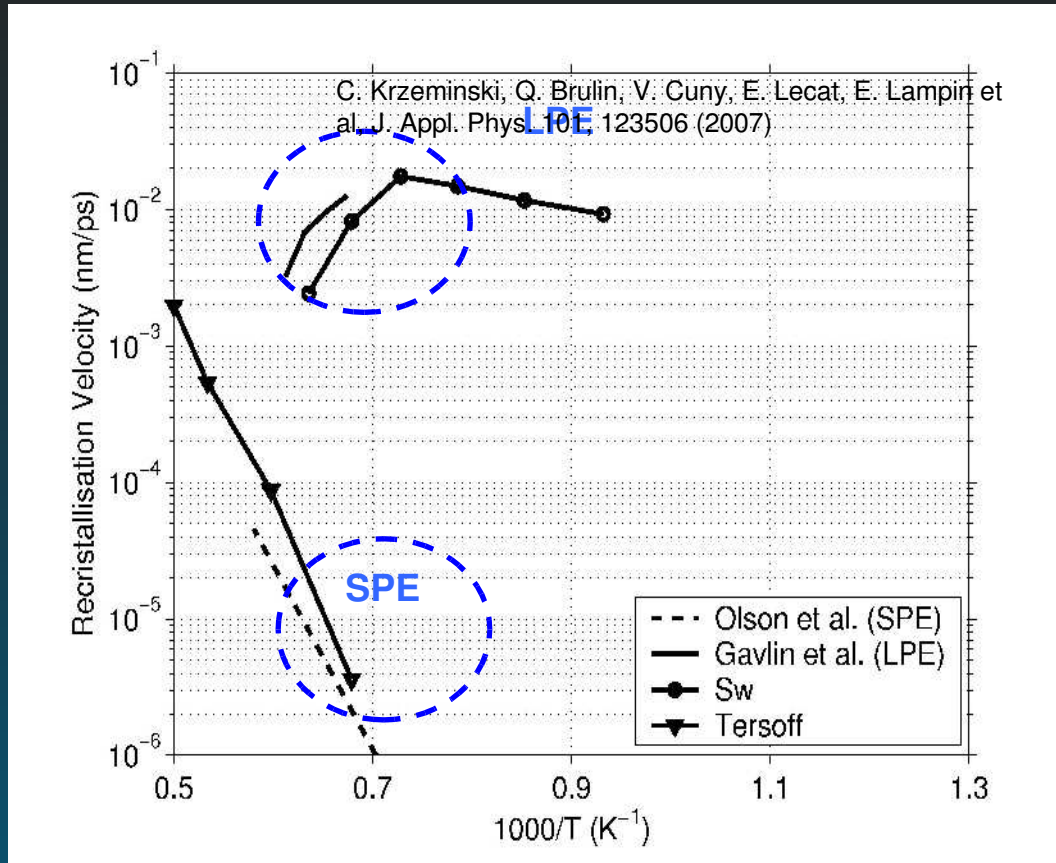


Extraction of the position of the interface vs time

# Molecular dynamics of SPE, LPE regrowth (2)

Conclusion :

Analysis of the velocities of recrystallization and of the structure of disordered part :



Potentiality to simulate both SPE and LPE

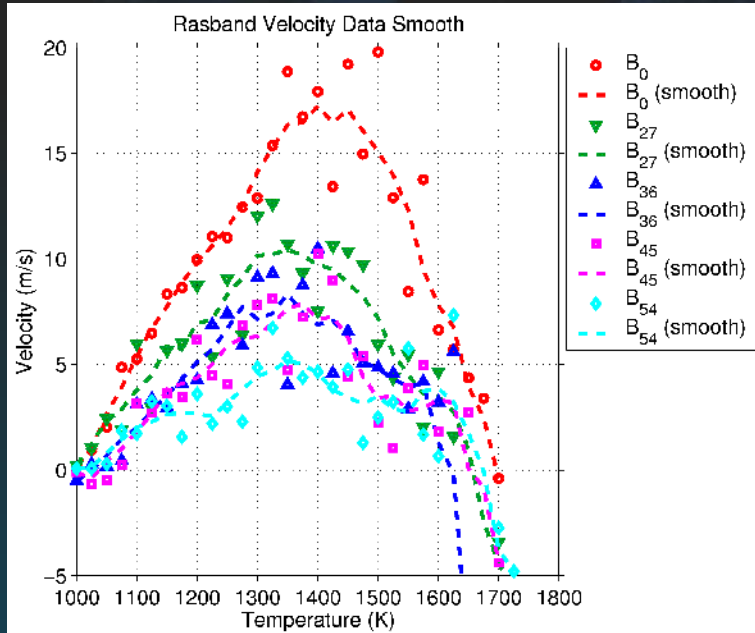
SPER or flash annealing

Laser annealing

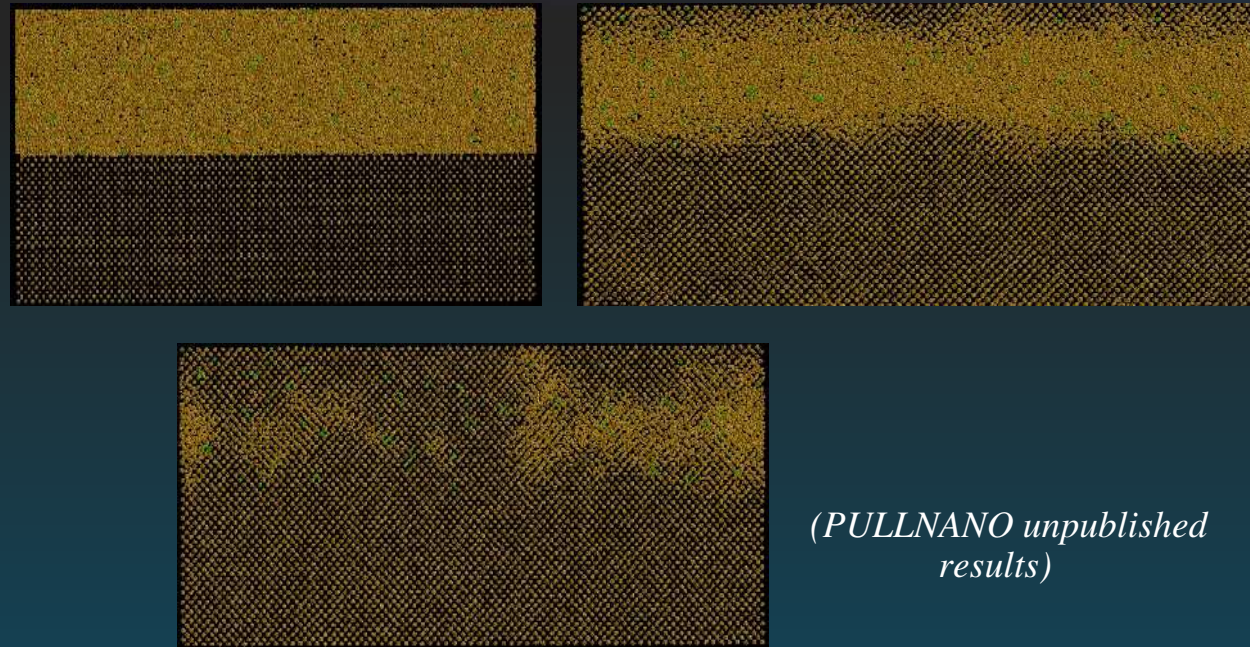
(PULLNANO results)

# Boron doped LPE regrowth

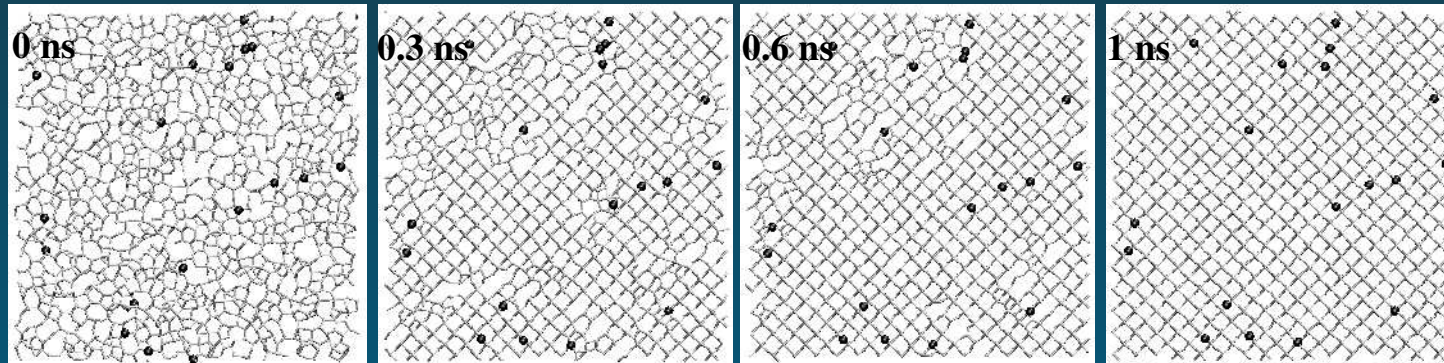
## Reduction of the velocity for large B concentration



## Interface roughening & amorphous pockets



## Incorporation of boron atoms in c-Si

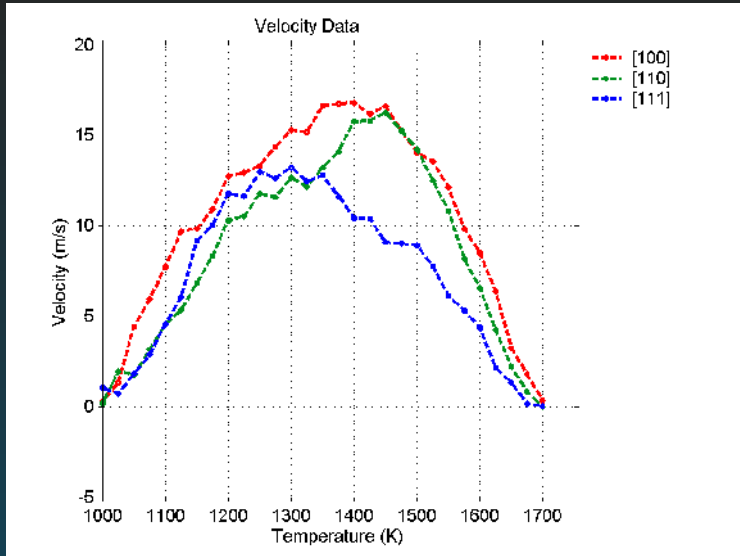


A. Mattoni and L. Colombo,  
Phys. Rev. B 69 (2004) 045204

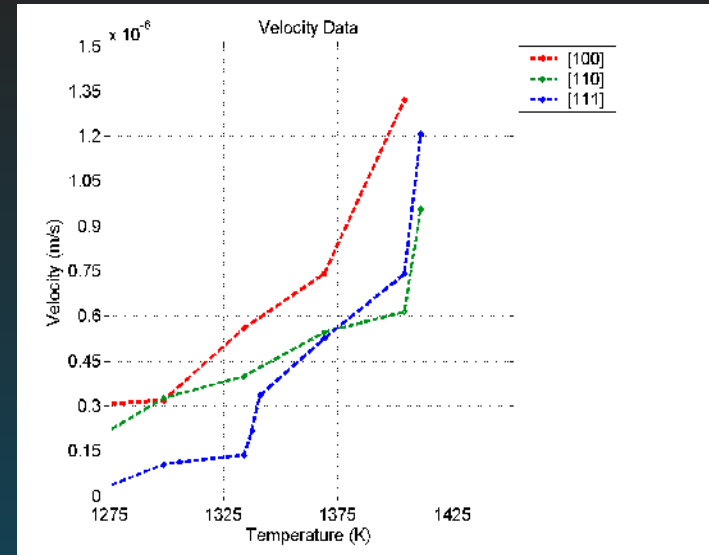
PULLNANO



# LPE or SPE: influence orientation effects



Orientation influence for LPE  $[100] > [110] > [111]$



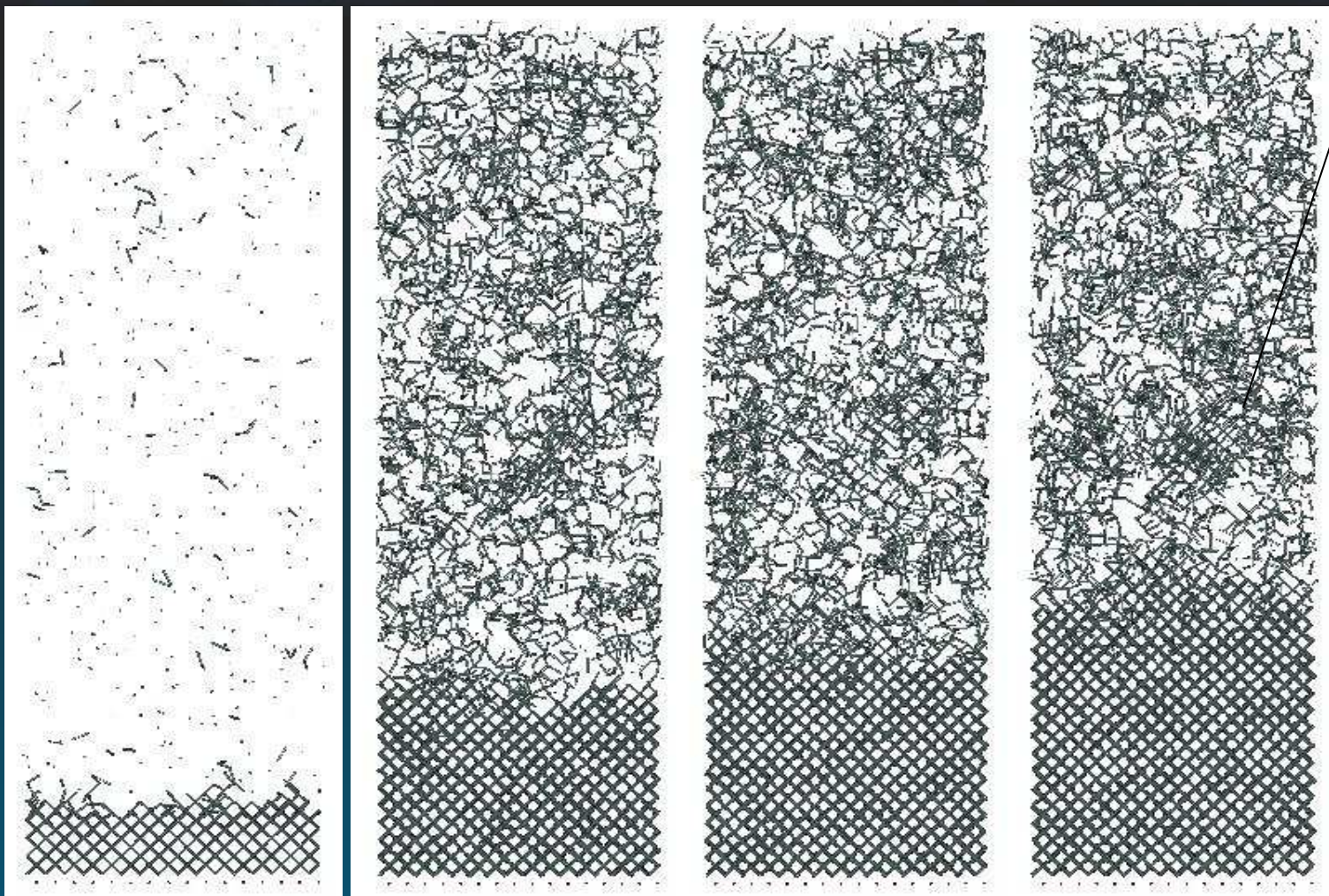
Orientation influence for SPE  $[100] > [110] > [111]$

*(PULLNANO unpublished results)*

# Competition SPE/RNG

Thick amorphous layer

Some grains begin to form by RNG



Thin crystalline germ

30 ns

60 ns

80 ns

Crystallization has progressed by SPE

(PULLNANO unpublished results)