



Process simulation for advanced stress and junction engineering

Christophe Krzeminski, Evelyne Lampin

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Christophe Krzeminski, Evelyne Lampin. Process simulation for advanced stress and junction engineering. École thématique. ESSDERC/ESSCIRC 2008 Tutorial Session T2 Nanoelectronics : Characterisation for the nanoelectronics era, Edinburgh, UK, 2008, 53 p. cel-00667574v2

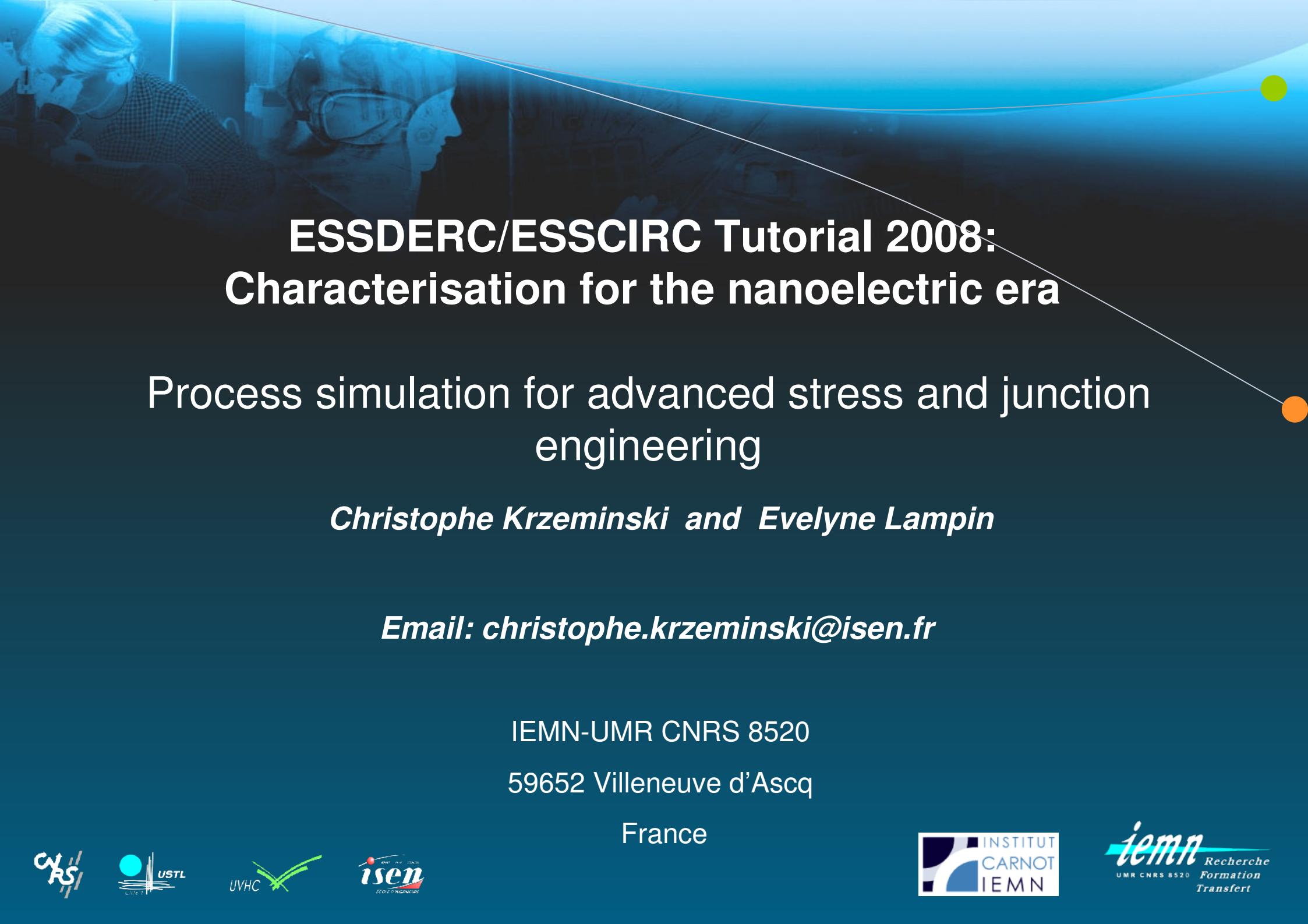
HAL Id: cel-00667574

<https://cel.hal.science/cel-00667574v2>

Submitted on 8 Feb 2012

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ESSDERC/ESSCIRC Tutorial 2008: Characterisation for the nanoelectric era

Process simulation for advanced stress and junction
engineering

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59652 Villeneuve d'Ascq

France



Tutorial objectives

“Process simulation for advanced stress and junction engineering »

» Large topic and only 45 minutes !

» and 53 slides

» Why Simulation in a characterisation tutorial ?

» Complementary...

» Not a so good idea to go deeply in the modeling aspect

» Overview of the field: the challenge (Part I), status (Part II), progress (Part III & IV) and perspectives (Part V)

» No equation



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Outline

Part I: Introduction: Challenge and solution for downscaling

Part II: Process simulation ?

Part III: Recent progress in the modeling of stress

Part IV: Recent progress in the modeling of junction engineering

Part V: Perspectives in Atomistic TCAD: towards some atomistic experiment ?



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Part I Introduction: Challenge and solution for downscaling

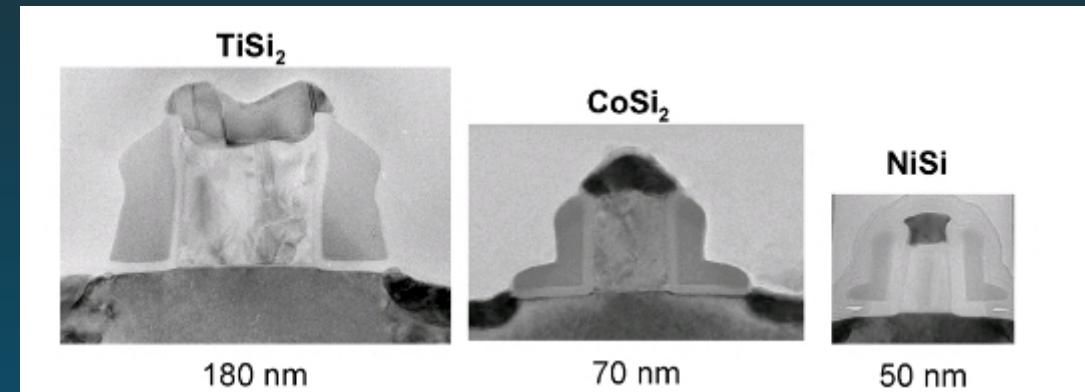
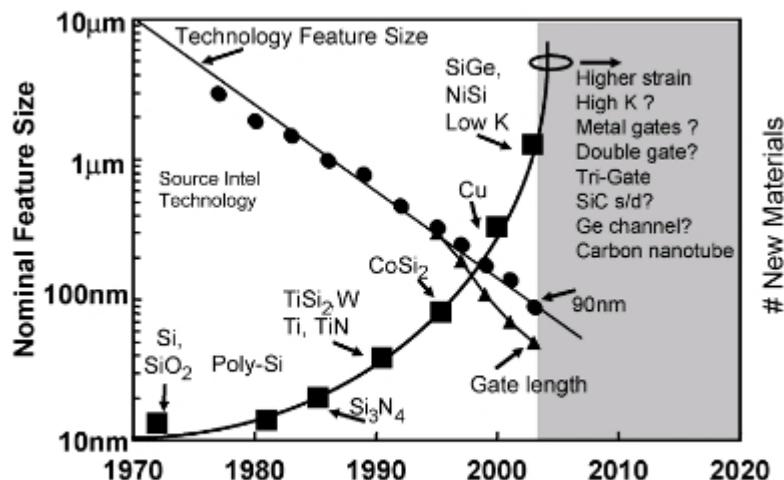
Downscaling ($\rightarrow 90$ nm)

26

IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 18, NO. 1, FEBRUARY 2005

In Search of “Forever,” Continued Transistor Scaling One New Material at a Time

Scott E. Thompson, *Senior Member, IEEE*, Robert S. Chau, *Senior Member, IEEE*, Tahir Ghani, Kaizad Mistry,
Sunit Tyagi, *Member, IEEE*, and Mark T. Bohr, *Fellow, IEEE*



S. E. Thompson et al., *IEEE Trans. On Semiconductor Manufacturing*, Vol. 18, n°1, 2005

Downscaling ($\rightarrow 90$ nm)

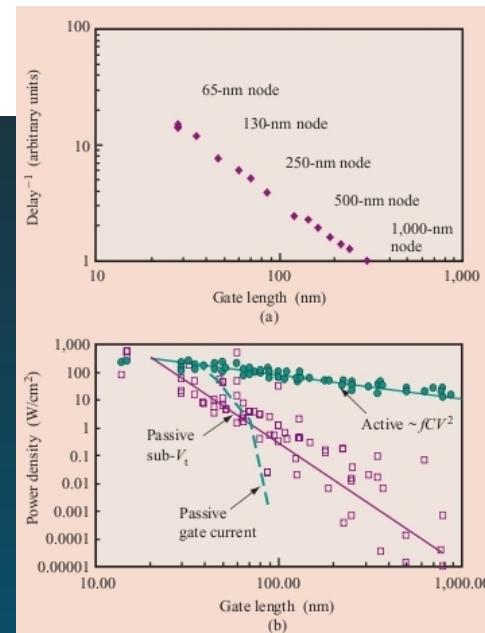
Silicon CMOS devices beyond scaling

To a large extent, scaling was not seriously challenged in the past. However, a closer look reveals that early signs of scaling limits were seen in high-performance devices in recent technology nodes. To obtain the projected performance gain of 30% per generation, device designers have been forced to relax the device subthreshold leakage continuously from one to several $nA/\mu m$ for the 250-nm node to hundreds of $nA/\mu m$ for the 65-nm node. Consequently, passive power density is now a significant portion of the power budget of a high-speed microprocessor.

Table 1 Relationships for constant-field scaling and for generalized field scaling. α is the scaling factor for dimensions, and $E = V/\alpha$ is the normalized electric field.

Parameter	Constant-field scaling	Generalized field scaling
Physical dimensions, L, W, T_{ox} , wire pitch	$1/\alpha$	$1/\alpha$
Body doping concentration	α	E/α
Voltage	$1/\alpha$	E/α
Circuit density	$1/\alpha^2$	$1/\alpha^2$
Capacitance per circuit	$1/\alpha$	$1/\alpha$
Circuit speed	α	α (goal)
Circuit power	$1/\alpha^2$	E^2/α^2
Power density	1	E^2
Power-delay product (energy per operation)	$1/\alpha^2$	E^2/α^3

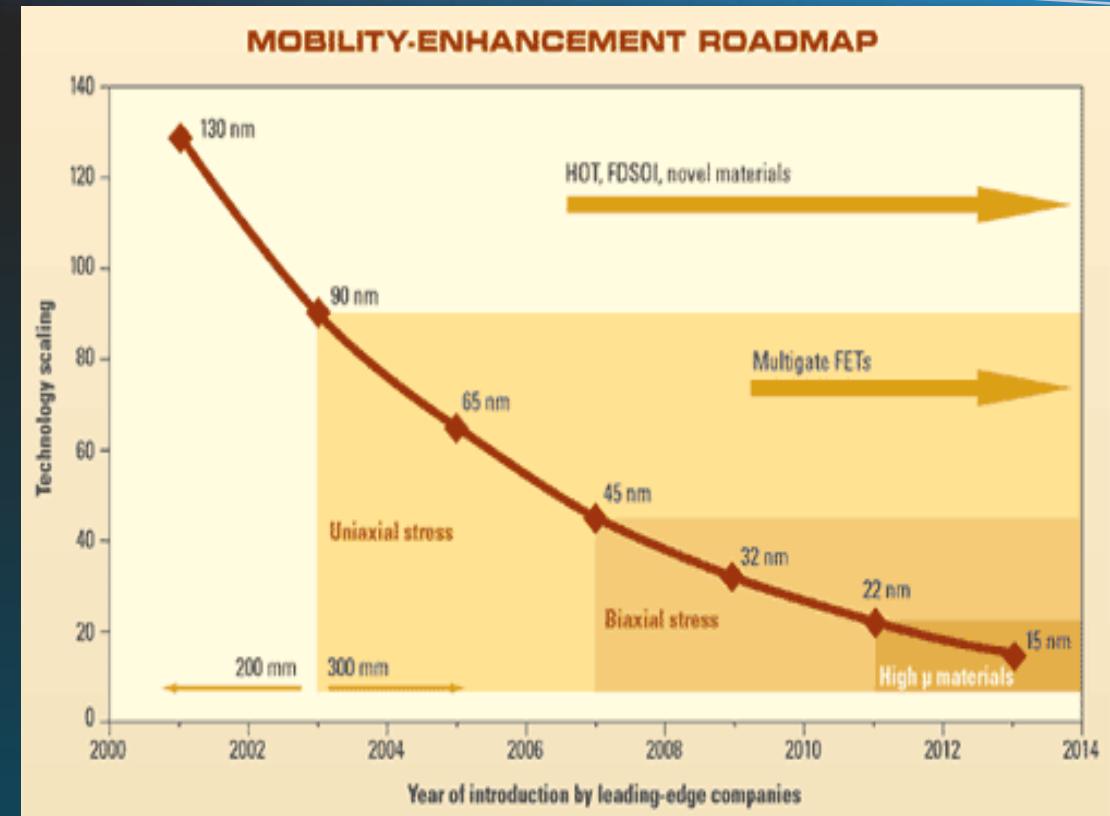
W. Haensch
E. J. Nowak
R. H. Dennard
P. M. Solomon
A. Bryant
O. H. Dokumaci
A. Kumar
X. Wang
J. B. Johnson
M. V. Fischetti



W. Haensch et al., IBM J. Res&Dev, Vol. 50, n°45, 2006

Stress Engineering approach

- (90nm → ?)



Mohta et al., IEEE Circuits and Magazine 2005

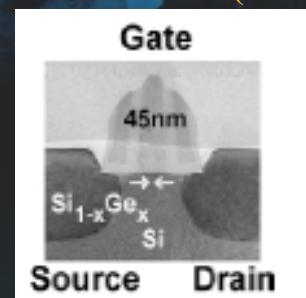
L. Peters, "Options Narrow at 45nm", Semiconductor International, 2006

Main idea: Strain engineering for enhanced mobility and drive current

Uniaxial stress techniques

PMOS

SiGe stressor (eSiGe)



T. Ghani et al., IEDM 2003

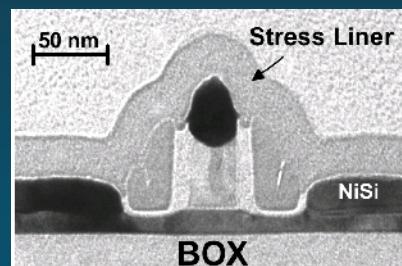
NMOS

Dual Stress Liner (DSL)



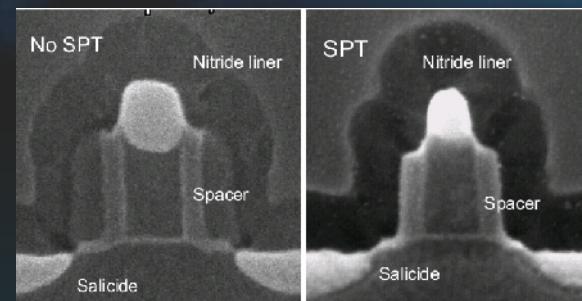
H. S. Yang et al., IEDM 2004

Stress Memorization (SMT)



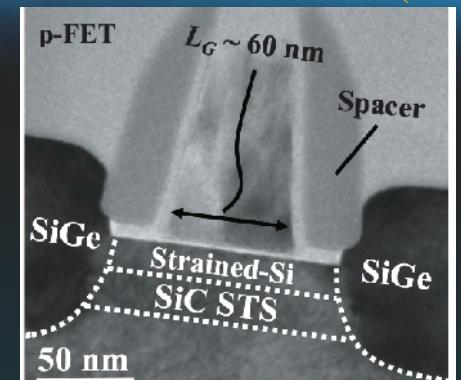
V. Singh et al., IEDM 2005

Stress Proximity Technique (SPT)



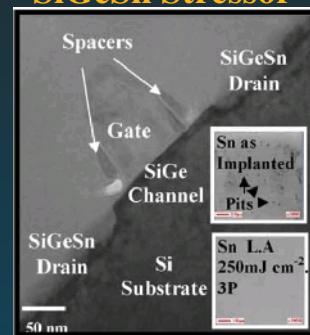
X. Chen et al., VLSI 2006

Strain Transfer Structure (STS)



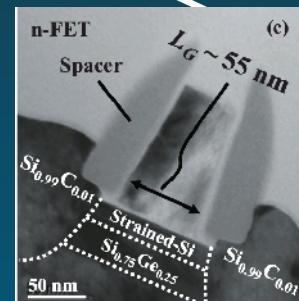
H. S. Ang et al., VLSI 2007

SiGeSn Stressor



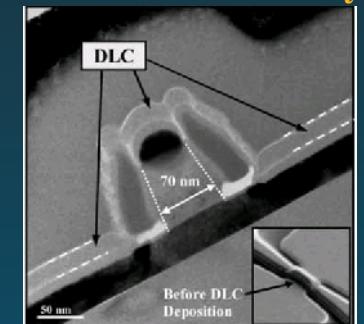
Wang, IEDM 2007

Strain Transfer Structure (STS)



H. S. Ang et al., VLSI 2007

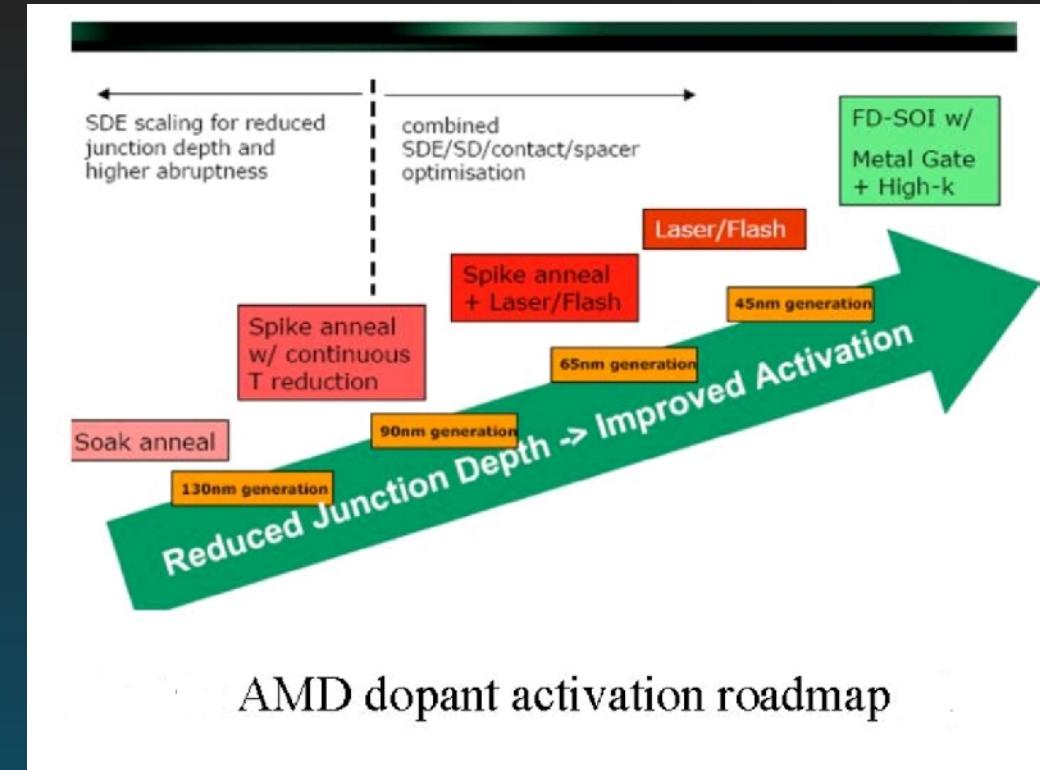
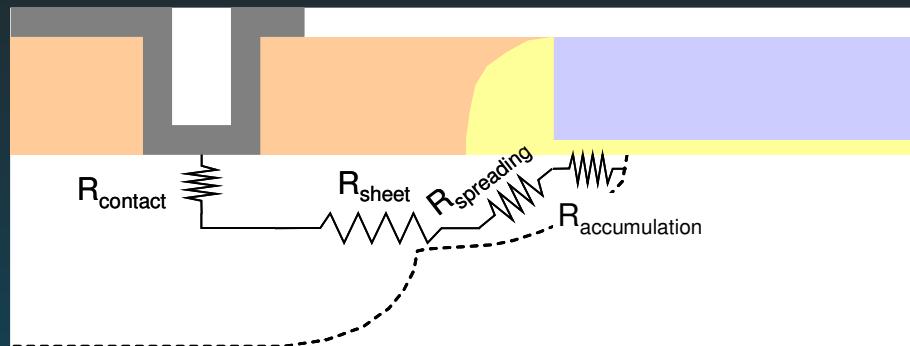
Diamond Like Carbon layer (DLC)



Tan, IEDM 2007

**Level of stress
in the channel**

Junction optimisation



R_{Sheet} : Conductivity of high doped region
High activation: complex techniques

J. O. Borland, « 32 nm NODE USJ Implant & Annealing, RTP 2007 »

Challenges for 32 & 22 nm

Challenges and Opportunities for High Performance 32 nm CMOS Technology

J.W. Sleight, I. Lauer, O. Dokumaci, D. M. Fried, D. Guo, B. Haran, S. Narasimha, C. Sheraw, D. Singh, M. Steigerwalt, X. Wang, P. Oldiges, D. Sadana, C.Y. Sung, W. Haensch, and M. Khare
IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights NY 10598
sleight@us.ibm.com (914) 945-1876

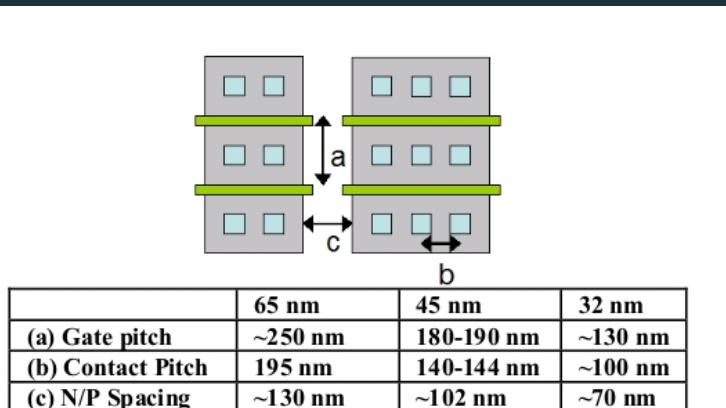


Fig. 1: Selected critical dimensions for different technology nodes.

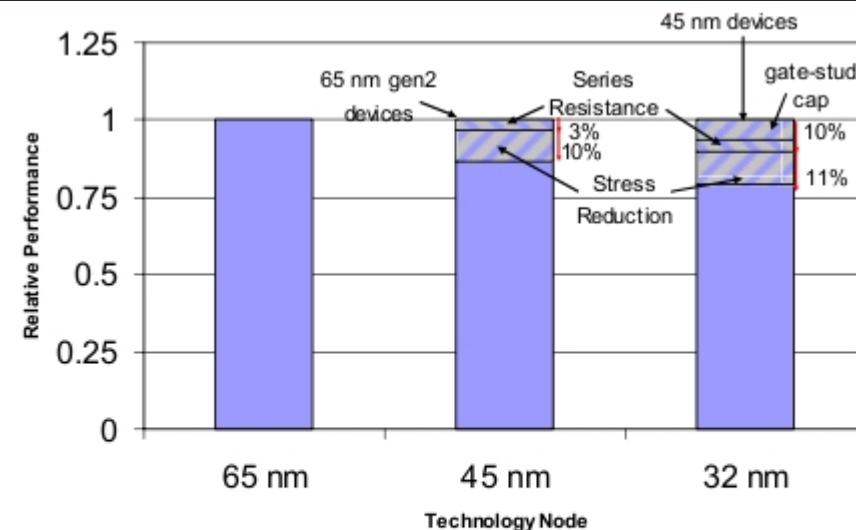


Fig. 2: Performance loss associated with pitch scaling for the 45 nm and 32 nm nodes. The performance loss associated with parasitics and stress loss is likely exacerbated at the 32 nm node.

J. W. Sleight et al., IEDM Tech. Dig., 2006

Challenges for 32 nm

- Scalability:
 - -11% stress reduction compared to 65nm (decreasing gate pitch) [Sleight06]
 - ITRS Junction target (extension depth, abruptness& sheet resistance) challenging
- Yield:
 - ITRS[07] : integration of multiple sources of local and global stress
 - Not exceeding the local critical shear stress
- Design
 - Pitch and layout dependent
 - “*Strain adds new challenges from a design perspective*” [Lammers08]

→ TCAD have a role to play to provide key information (process => design)



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PART II

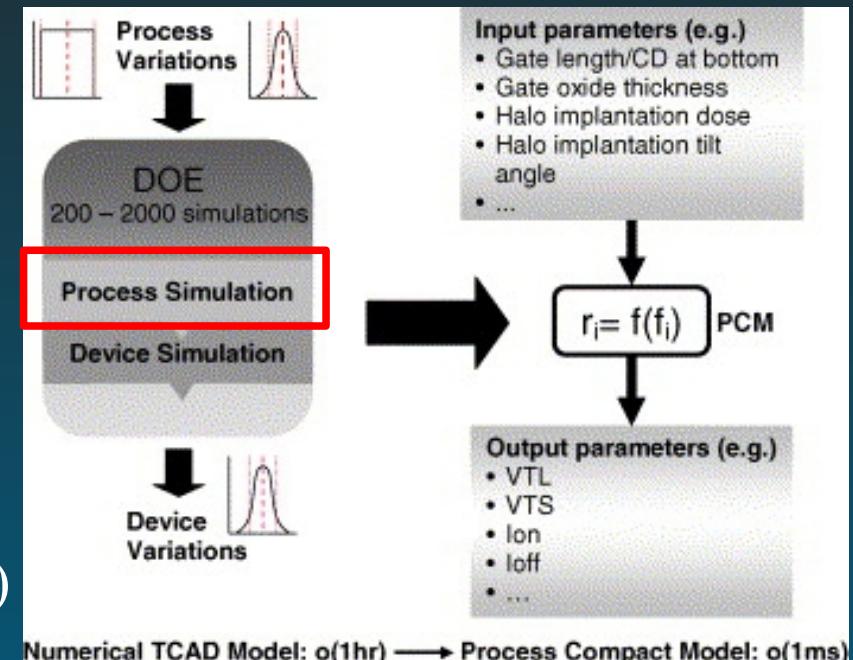
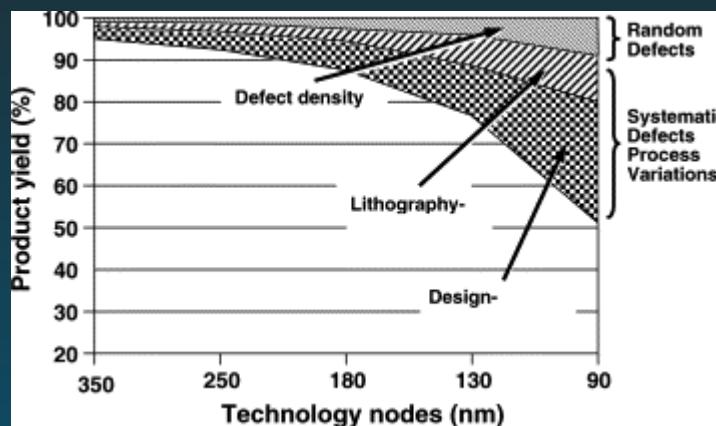
PART II: Process Simulation ?



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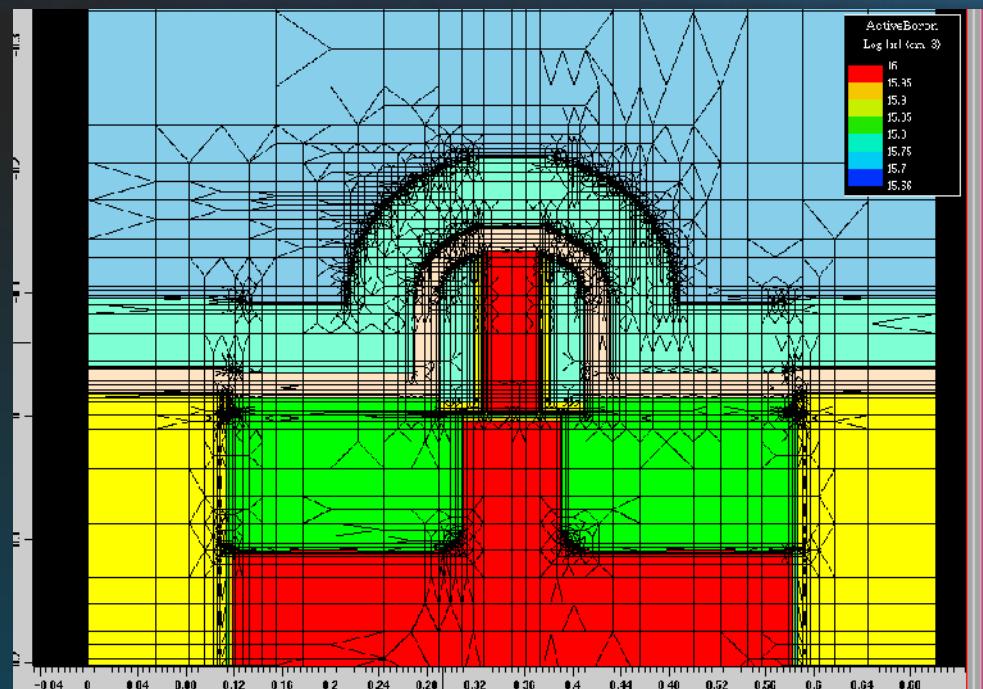
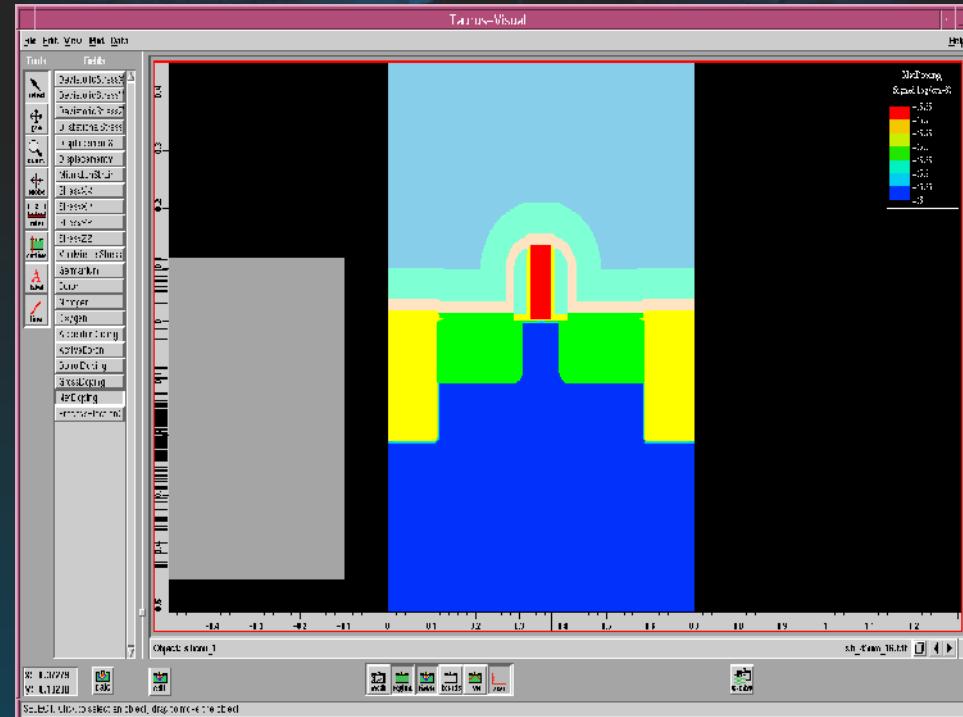
TCAD ?



TCAD:

- ↘ Technology cost development (40% ITRS)
- ↗ Yield

Process Simulation



Standard process simulation:

- Transistor Building (finite elements)
- Simulation of the various process step (implantation, diffusion, oxidation, silicidation)
- « Physical » modeling with partial differential equations (PDE)
- Knowledge of the various physical parameters (topology, dopant distribution, stress field) for electrical simulation

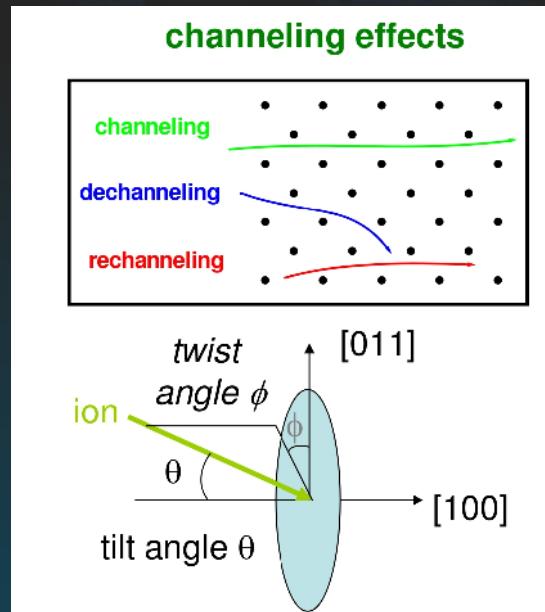


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Implantation modeling

Implantation modeling : Implant tables or Monte-Carlo Simulation



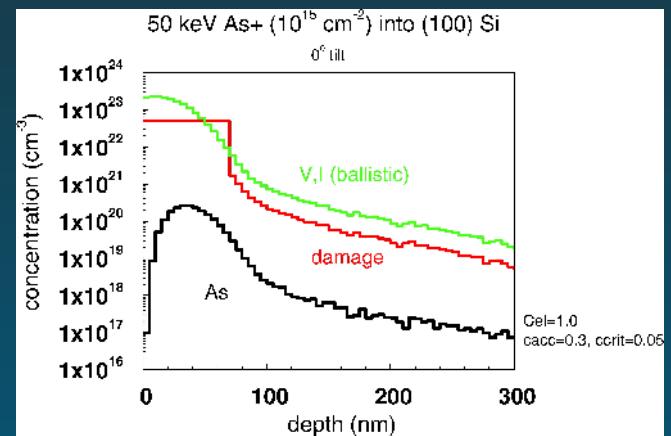
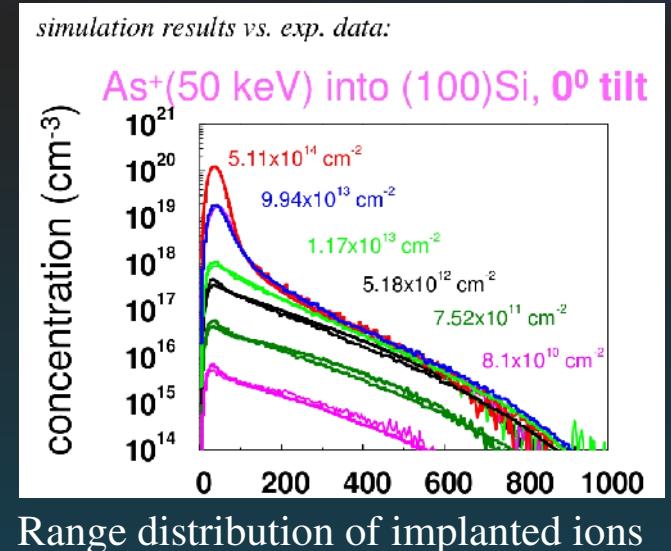
Series of consecutive binary collisions of the projectile with the lattice (BCA MC):

Nuclear scattering (Coulomb pair potential)

Semi empirical model for the electronic energy loss of particles

Phenomenological models for damage probability

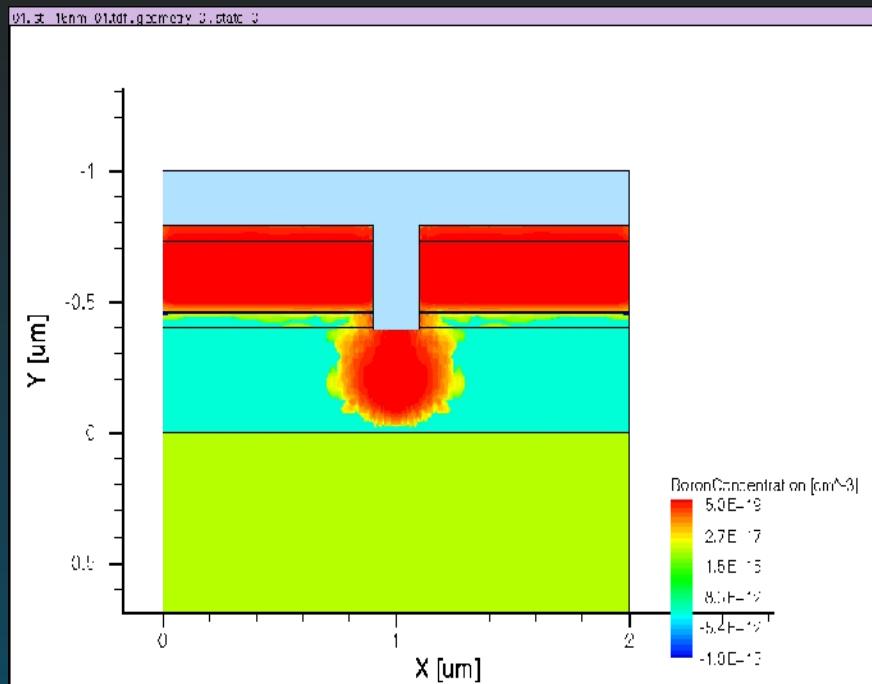
M. Posselt, private communication



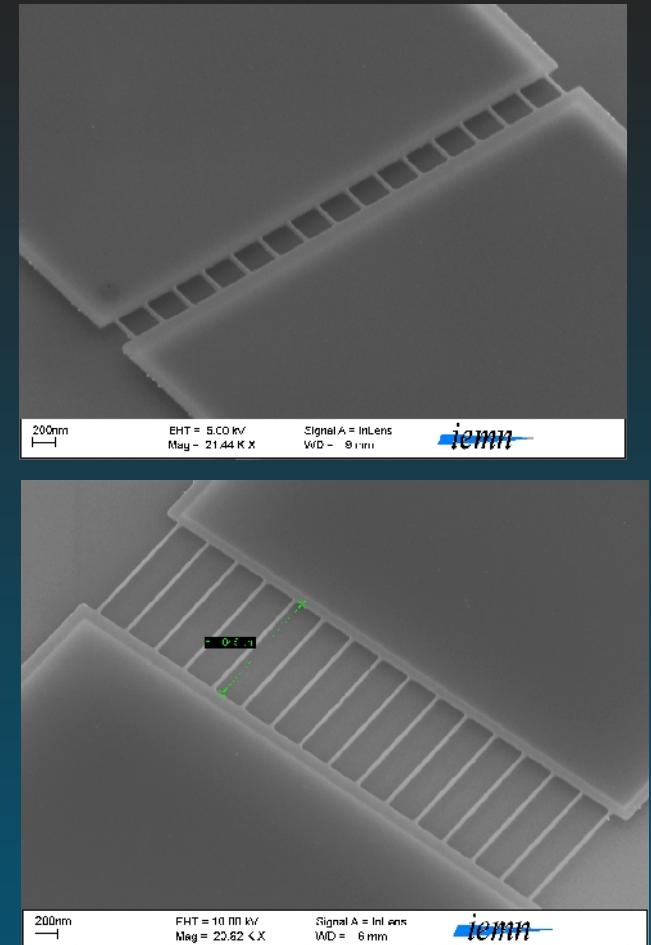
Damage profile

Implantation Modeling Example

- 2D Implant modeling for nanowire fabrication



Creation of Silicon nanowire by anisotropic etching with a damage gradient
Optimisation (Dopant, Dose, Energy) with simulation



Vikram Passi et al., UCL, NANOSIL WP 2.1 (unpublished results)



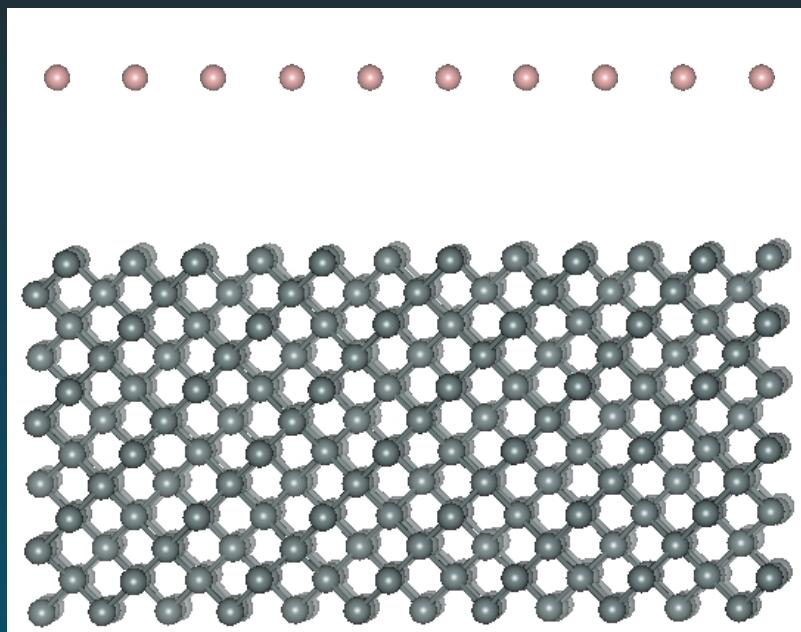
Diffusion modeling (1)

Junction Fabrication

Standard Technology

Ionic implantation for the dopant with various energy& dose

Boron atoms



After implantation:

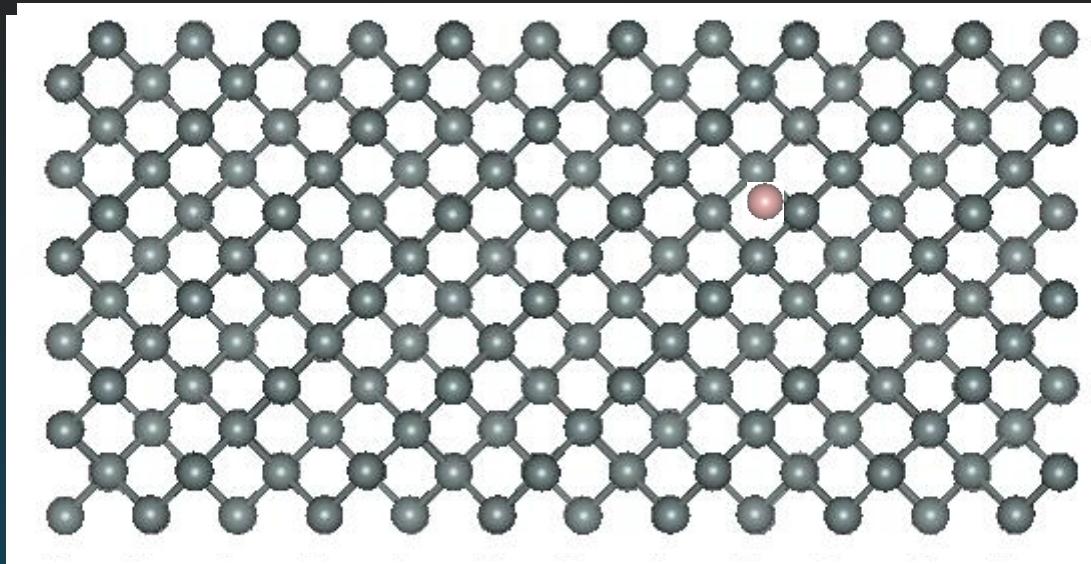
- Dopants in an interstitial position electrically inactive
- Defects created : interstitials, vacancies, aggregate, amorphous pocket

→ Annealing step mandatory

Diffusion Modeling (2)

Boron Kick-out

What's going on during annealing? Example for boron

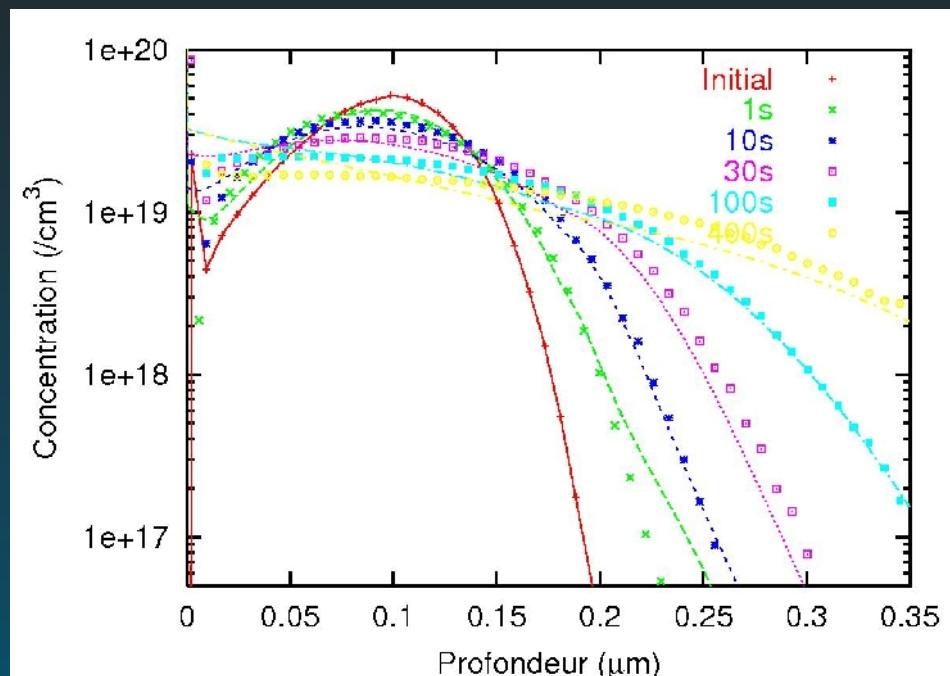


- The junction depth and the activated dose results from the contribution of all these mechanisms
- Standard process simulator used Fick law and diffusion-reaction equations to describe the interaction with point defects and mechanism like kick-out

- Interstitial Boron mobile form
- Immobile Boron impurity (electrically active) and creation of Si interstitial
- Diffusion and recombination of Si interstitial.
- Kick-out of a boron atom by an another Si interstitial
- ...

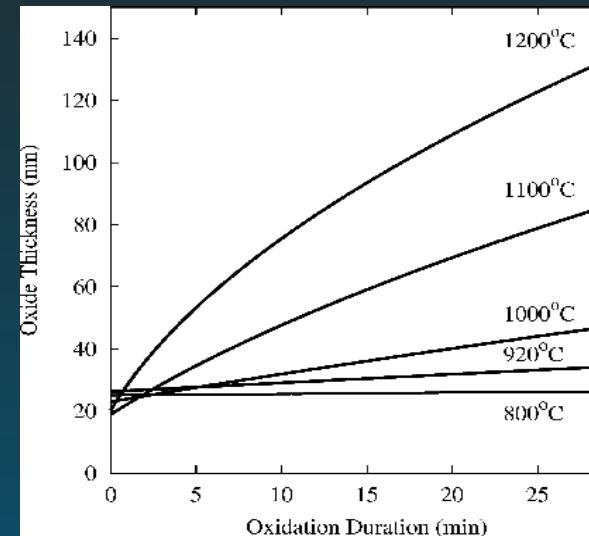
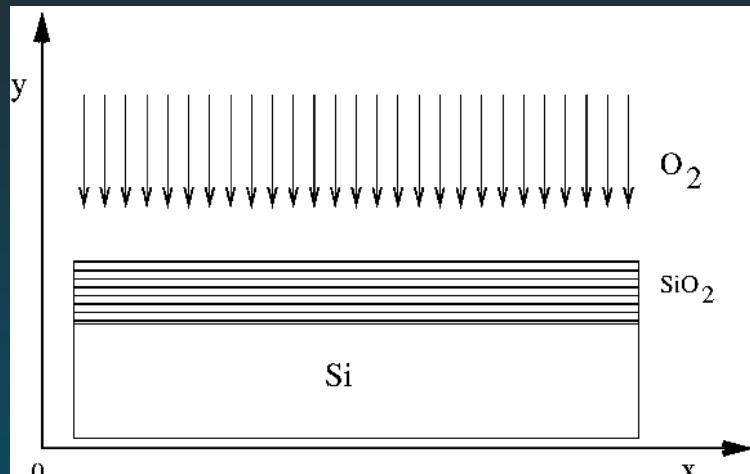
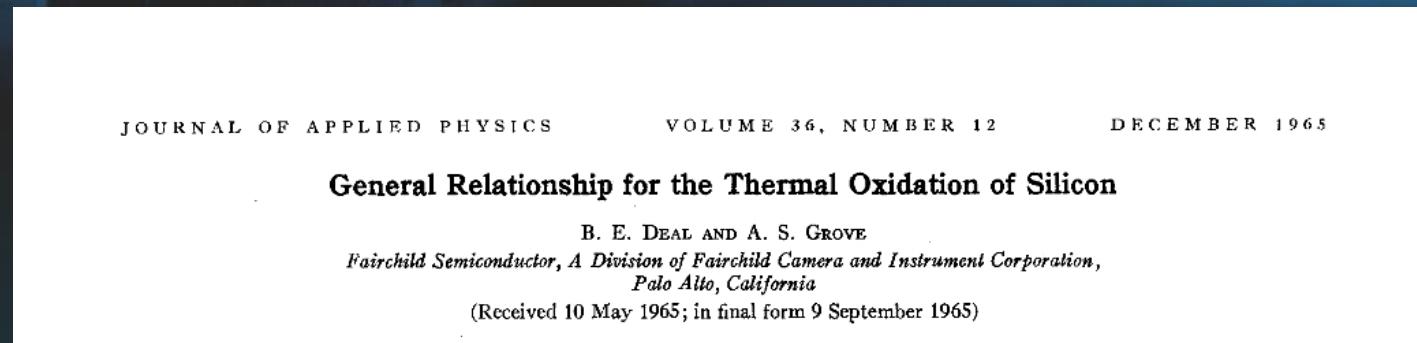
Diffusion Modeling (3) ●

- Application: Evolution of doping profile during annealing critical for electrical properties (see also slide 44)



Example of Boron diffusion profile diffusion

Oxidation and stress modeling (1)

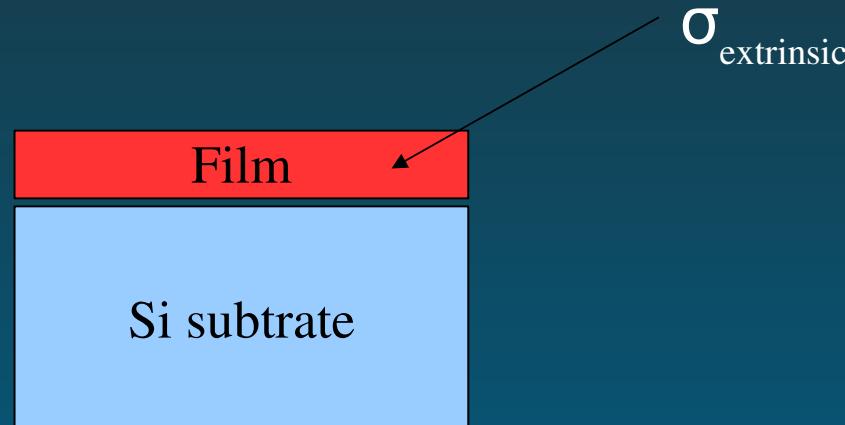


Process simulator : generalised Deal&Grove oxidation model (diffusivity & and reaction rate stress-dependent) to take into account the stress (volume expansion)

Various source of stress

Stress sources	Technical Process
Thermal Stress	Thermal variation during various processing step
Topological induced Stress	Thermal growth (oxidation, silicidation), etching
Intrinsic Stress	Film deposition process (nitride, polysilicon, metals....)
Extrinsic stress	Structural modifications of films
High doping induced stress	Steep doping gradients

Example : modeling of stress generated by deposition of thin film
introduction of an extrinsic stress and mechanical equilibration



Example: Oxidation and stress modeling

JOURNAL OF APPLIED PHYSICS

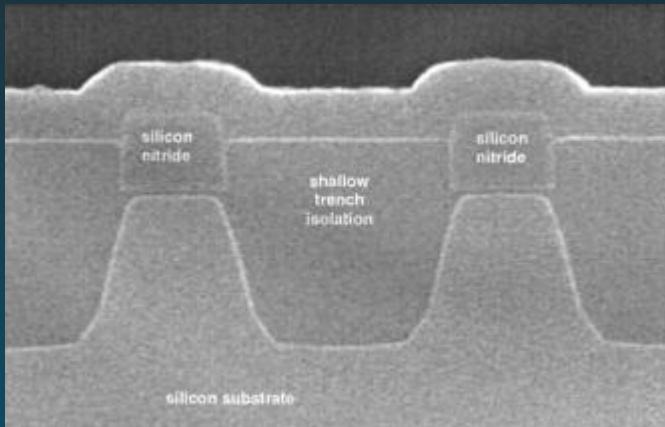
VOLUME 94, NUMBER 9

1 NOVEMBER 2003

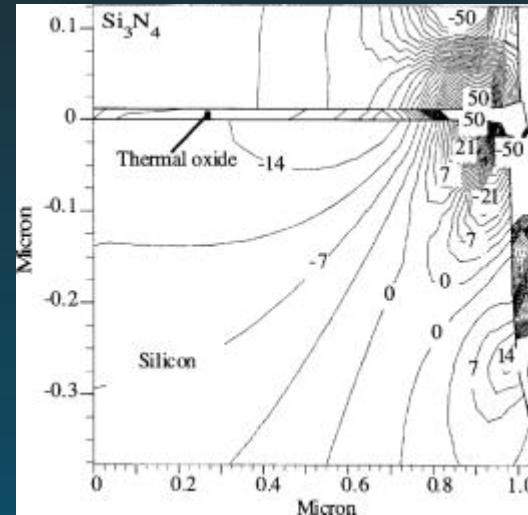
Strain determination in silicon microstructures by combined convergent beam electron diffraction, process simulation, and micro-Raman spectroscopy

Vincent Senez^{a)}

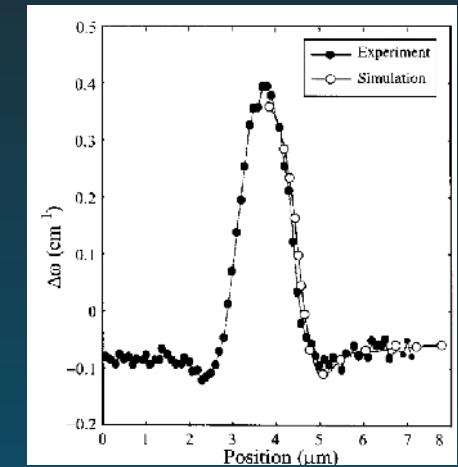
IEMN-ISEN, UMR CNRS-8520, Avenue Poincaré, B.P. 69, 59652 Villeneuve d'Ascq cédex, France



STI (Shallow stress Isolation structure)



Stress field (TCAD)



μRS (experiment vs simulation)
but for Large structure



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Conclusion

- These different examples => process modeling promising
- Reality is/was more complex (2002)
 - Example taken from different or academic softwares
 - Difficulty to describe TED Boron, segregation effects, ultra-thin oxidation, silicidation....
 - No real stress modeling capabilities (commercial tool)
- The Mark Law definition: « **TCAD : yesterday's technology modeled tomorrow**»



M. E. Law, IBM J. Res. Dev., Vol. 46, n°2/3, March 2002

Conclusion.

- « **TCAD : yesterday's technology modeled tomorrow**» still true ?
- No:
 - Large progress have been performed in diffusion modeling (Support by the EC: European project Rapid, Frendtech, PullNaNo, Atomics)
 - Progress have been done for « simple » stress modeling
 - The merging of the major TCAD firms (Avant!, ISE, Synopsys) ~ market 80% DIOS (meshing, numerical stability), TAURUS (3D capabilities, Implantation, stress) and TSUPREM-IV (oxidation modeling) to the FLOOPS-ISE (new diffusion modeling)
 - More contribution and more insight with atomistic modeling
 - There is also a part of « dream »: simulation can not replace characterisation
 - Script models speed up the pipeline (M. Law) : University (models)=>TCAD company (software) => Semiconductor Company ? No but more
- Yes:
 - Complexity increase : Stress Engineering (Slide 8), New material (Ge), Laser Annealing & Solid Phase Epitaxy.....

PART III

Recent progress in the modeling of stress



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Modeling SiGe S/D stress field

APPLIED PHYSICS LETTERS 86, 023103 (2005)

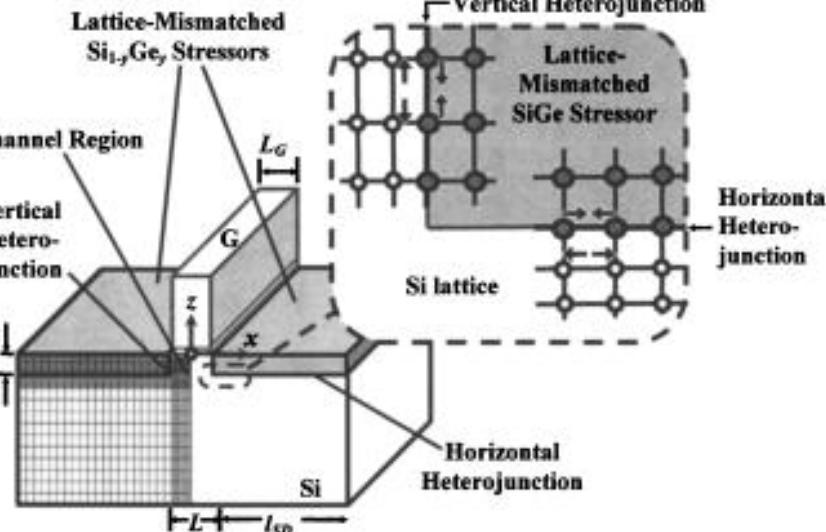
Finite-element study of strain distribution in transistor with silicon–germanium source and drain regions

Yee-Chia Yeo^{a)}

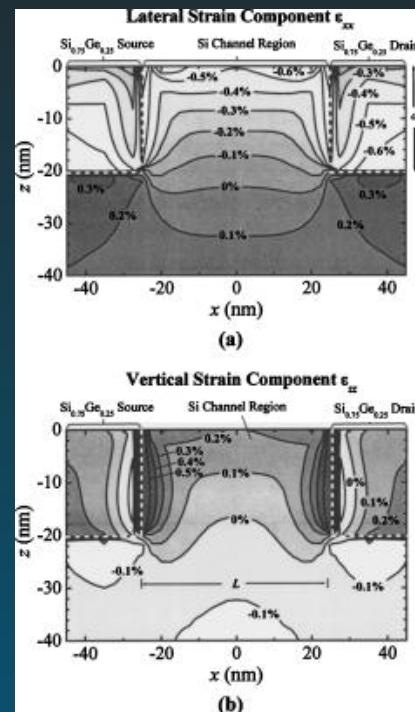
Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering,
National University of Singapore, 119260, Singapore

Jisong Sun

Agency for Science, Technology, and Research, Data Storage Institute, DSI Building,
5 Engineering Drive 1, 117608, Singapore



Principle of Lattice-mismatched stressor



Lateral & Vertical strain induced

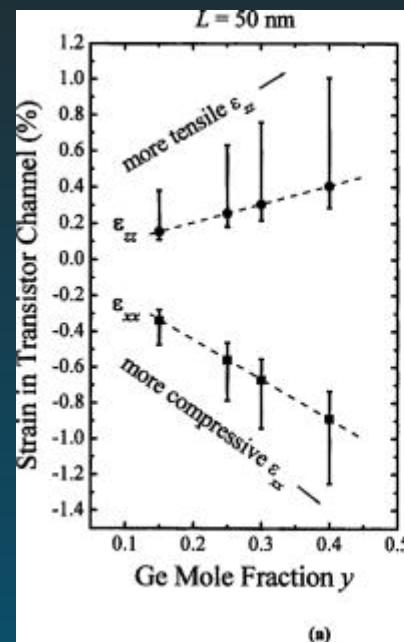
Y. Yeo et al., Appl. Phys. Lett., 86, 023103, 2005



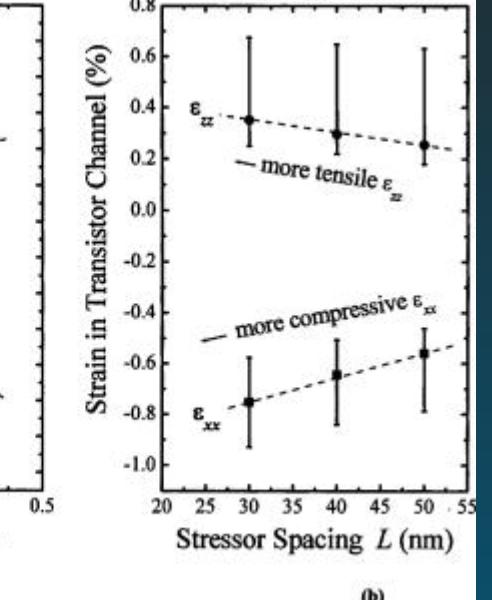
INSTITUT
CARNOT
IEMN



UMR CNRS 8520
Recherche
Formation
Transfert



Evolution of channel strain as a function of the Ge fraction and the spacer with



SiGe S/D scalability

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 7, JULY 2006

16/7

Scalability of the $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain Technology for the 45-nm Technology Node and Beyond

Geert Eneman, Peter Verheyen, Rita Rooyackers, Faran Nouri, *Senior Member, IEEE*, Lori Washington, Robert Schreutelkamp, Victor Moroz, Lee Smith, *Member, IEEE*, An De Keersgieter, Małgorzata Jurczak, and Kristin De Meyer, *Senior Member, IEEE*

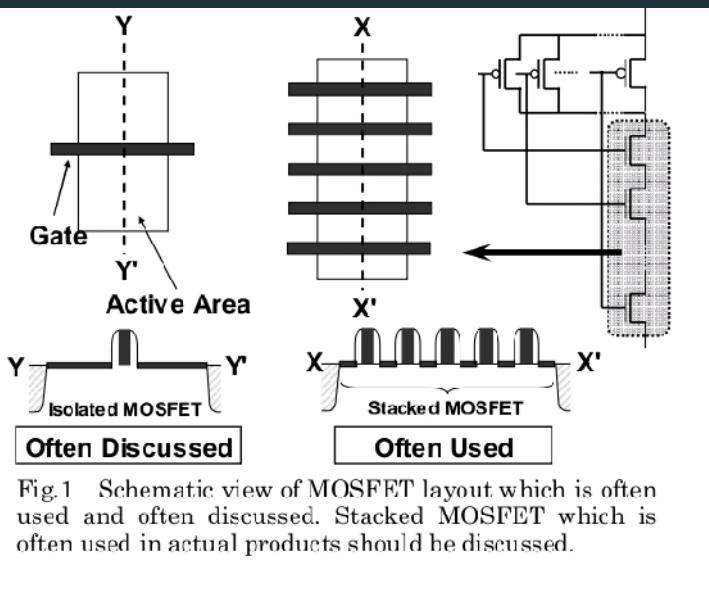
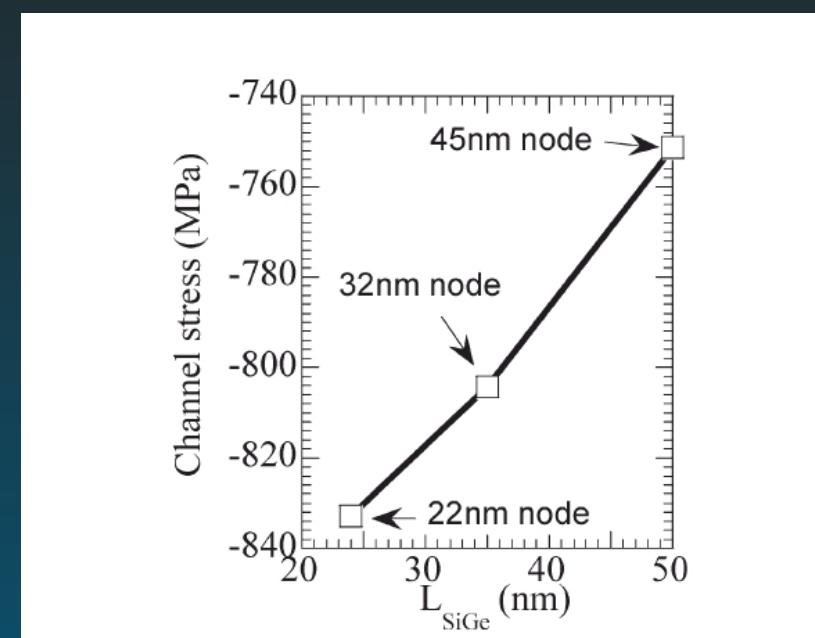
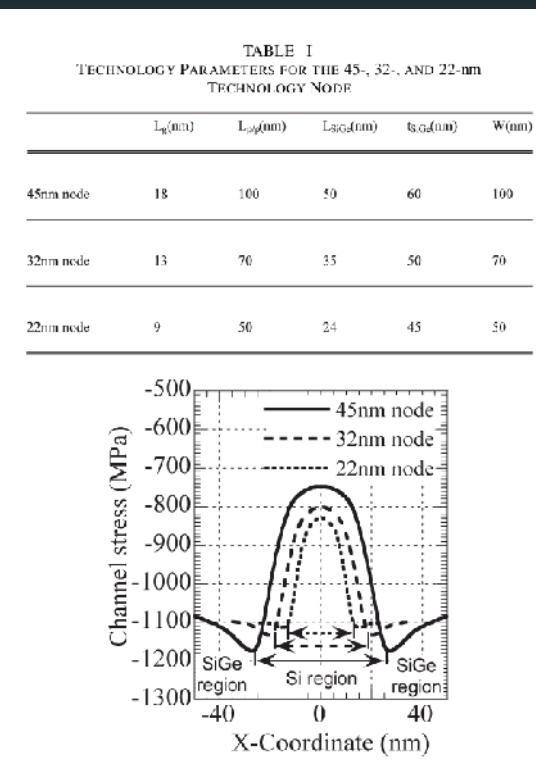


Fig. 1 Schematic view of MOSFET layout which is often used and often discussed. Stacked MOSFET which is often used in actual products should be discussed.



Mean compressive channel stress does not decrease with downscaling

G. Eneman et al., IEEE Trans. on Electron Device, Vol. 86, 023103, 2005

Modeling CESL stress

Multi-Layer Model for Stressor Film Deposition

K.V. Loiko, V. Adams, D. Tekleab, B. Winstead, X.-Z. Bo, P. Grudowski, S. Goktepeli, S. Filipiak, B. Goolsby, V. Kolagunta, and M.C. Foisy

Austin Silicon Technology Solutions, Freescale Semiconductor, Inc.
3501 Ed Bluestein Blvd. Austin, TX 78721
Email: loiko@freescale.com

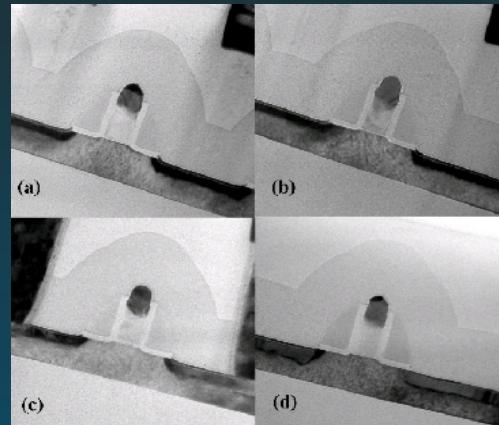


Figure 1. TEMs of 35nm gates with highly stressed ESL films as a function of gate poly pitch: (a) 0.26 μm , (b) 0.38 μm , (c) 0.63 μm , (d) 1.01 μm .

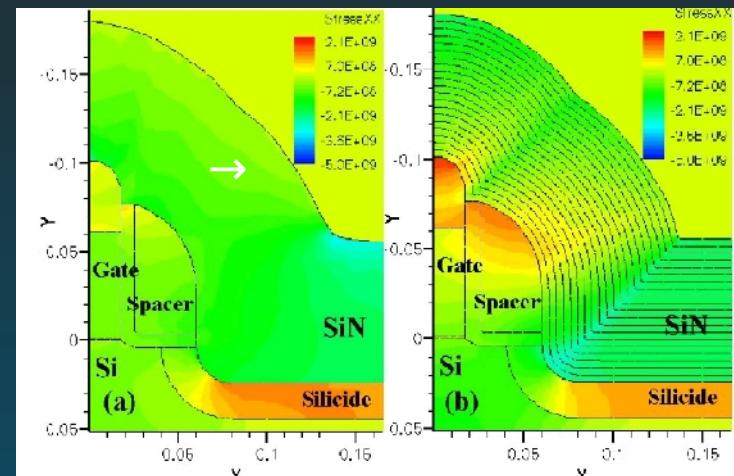


Figure 7. Contours of lateral stress (Pa) in 35nm transistor structures with 20nm source/drain recess simulated using (a) single-layer and (b) 20-layer deposition of nitride with compressive intrinsic stress.

Large difference between mono and multi step deposition

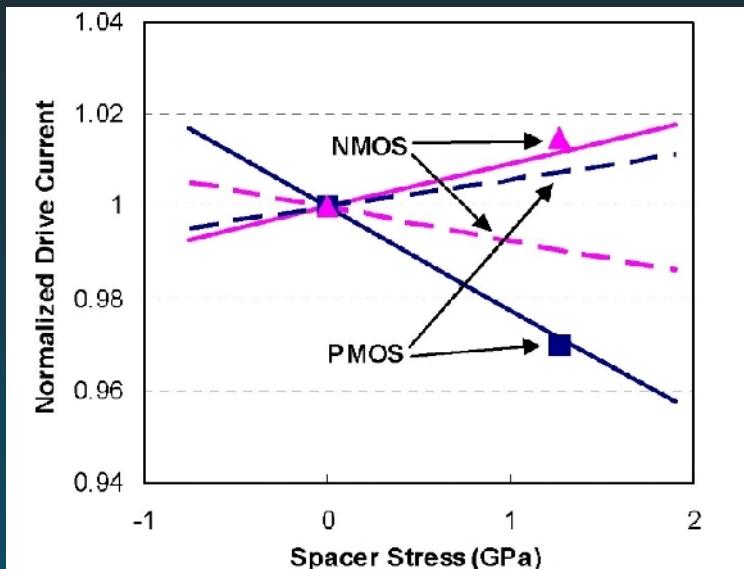


Figure 8. Experimental data (symbols), multi-layer (solid lines) and single-layer (dashed lines) simulation results on NMOS (tensile ESL) and PMOS (compressive ESL) drive current vs. spacer stress.

Opposite experimental trends with mono step deposition !

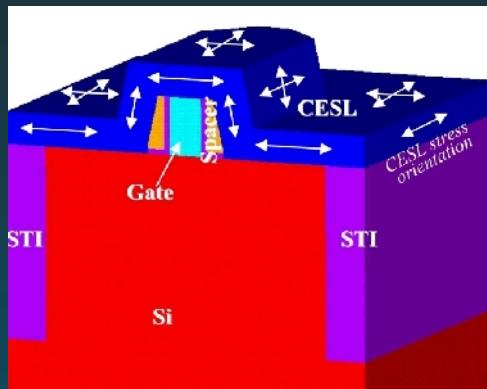
Engineering the CESL stress

814

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 4, APRIL 2007

Method for Managing the Stress Due to the Strained Nitride Capping Layer in MOS Transistors

Stéphane Orain, Vincent Fiori, Davy Villanueva, Alexandre Dray, and Claude Ortolland



3D Ansys Simulation

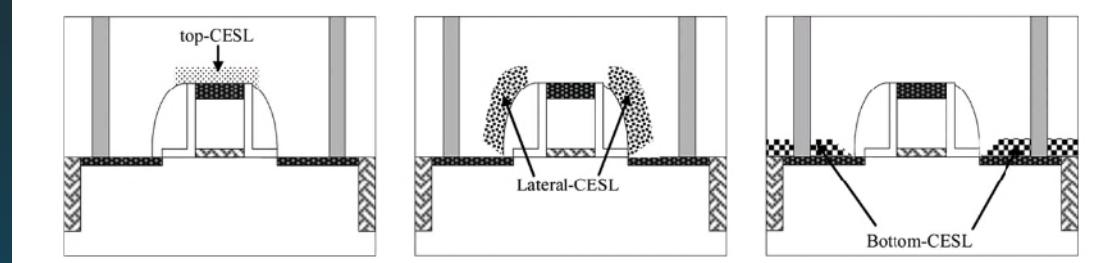


TABLE I
SUMMING UP THE IMPACT OF ALL THE CESL EFFECTS
(C = CORNER, D = DIRECT, AND I = INDIRECT) FOR EACH
CESL ZONE (TOP, LAT. — LATERAL, AND BOT. — BOTTOM)

		Corner	Top	Lat.	Bot.
Long	Sx	C+	D-	0	D+
	Sy	C+	D-	0	D+
	Sz	0	I-/D-	0	0
Short	Sx	C+	0	D-	D+
	Sy	C+	0	D-	D+
	Sz	0	I-	I-/D-	D-

LEGEND:

- C : Corner effects
- D : Direct effects
- I : Indirect effects
- : Compressive stress
- + : tensile
- 0 : no or low impact

Which part of the CESL influence the channel stress ?

- Complex answer (Long<>short device) !
- Such table provide guidelines for device optimisation
- Geometry of the spacer (L or D shape) important

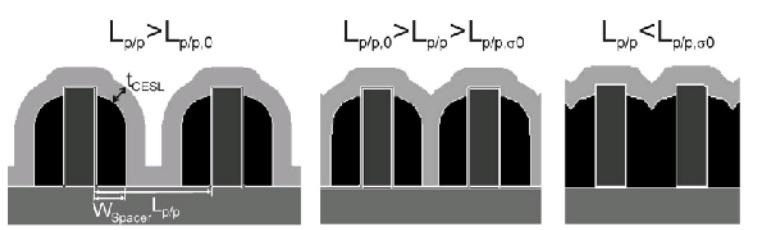
Scalability of CESL

1446

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 6, JUNE 2007

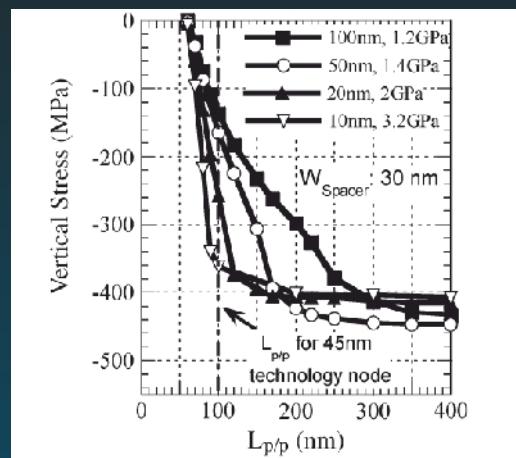
Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study

Geert Eneman, Peter Verheyen, An De Keersgieter, Małgorzata Jurczak, and Kristin De Meyer, Senior Member, IEEE

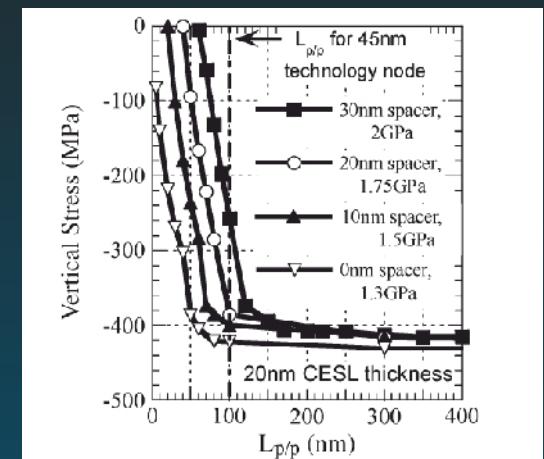


Poly to Poly Distance: $L_{p/p}$

$$L_{p/p} > L_{p/p,0} = 2 \cdot t_{CESL} + 2 \cdot W_{Spacer}$$



For large CESL thickness, decreasing $L_{p/p}$ leads to stress reduction

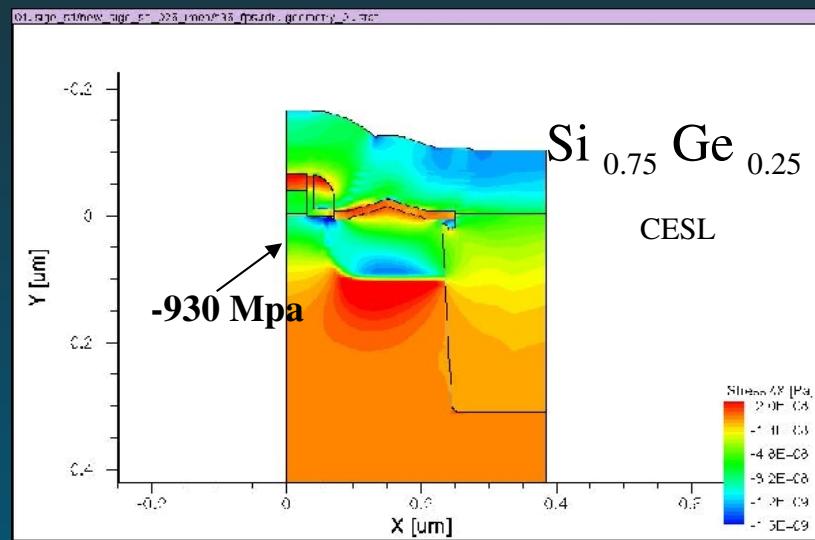
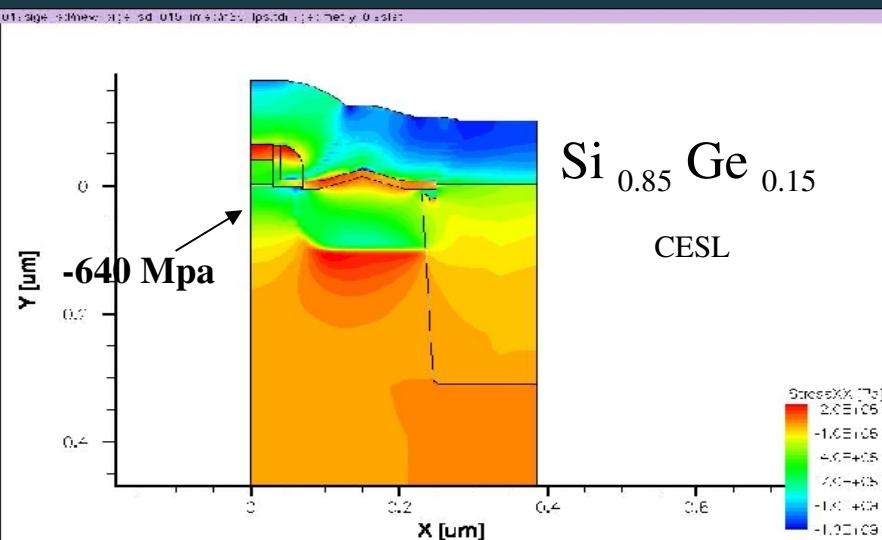
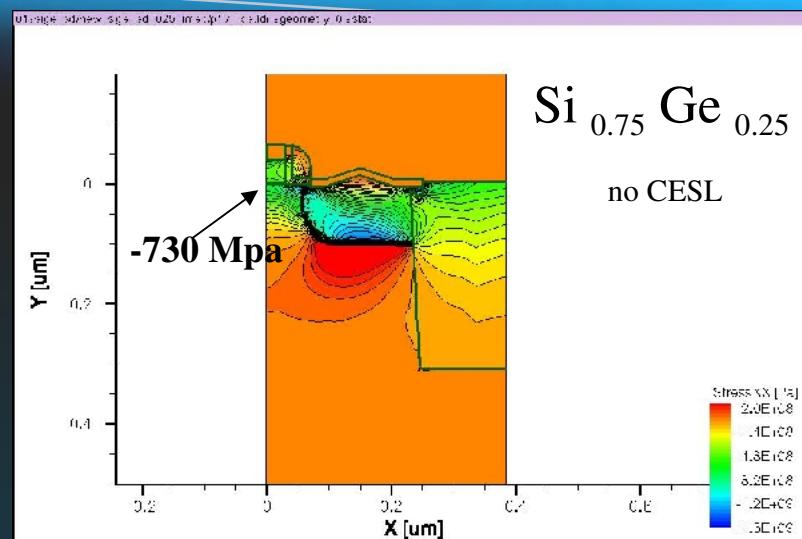
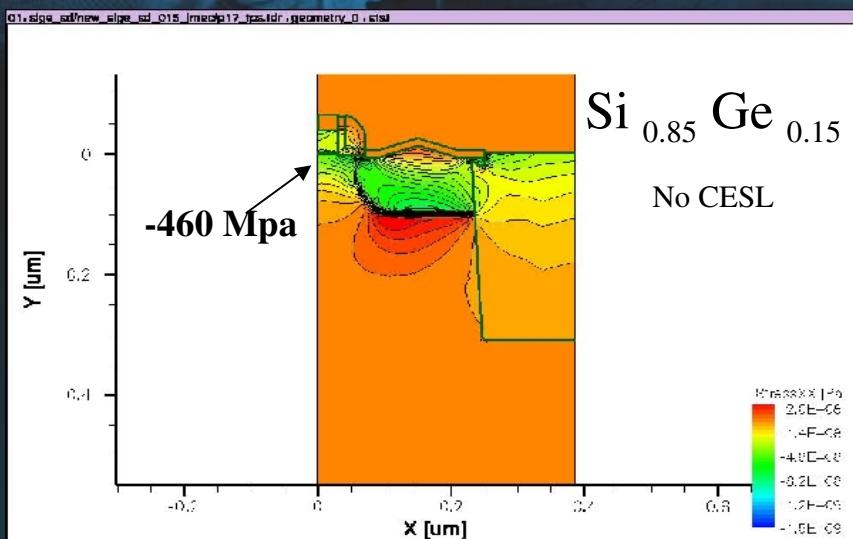


Influence of spacer width on vertical stress for decreasing $L_{p/p}$

↙ CESL thickness is no sufficient, spacer dimensions must be scaled

G. Eneman et al., IEEE Trans. on Electron Device, Vol. 54, N°6, June, 2007

S/D SiGe & CESL modeling with SProcess



C. Krzeminski , PULLNANO Results (unpublished)

Conclusion

- Large progress have been performed in the stress modeling with the support of experimental development, study of topography influence, evaluation of scalability (SiGe S/D or Stress Liner)
- There was one issue :

Journal or major proceedings conferences Publications (2001-2008)	Number	Proprietary simulator	"Old" simulator Taurus/ Tsuprem-IV	Mechanical simulator (Ansys/ FEMLAB)	Sentaurus Process
TCAD&stress	14	30%	40%	30%	0%

- But large progress have been performed recently in the last version of Sentaurus Process as shown by the last PullNANO Results
- Still a lot of work: Stress Memorization, SiC stressor.....

Progress in diffusion modeling

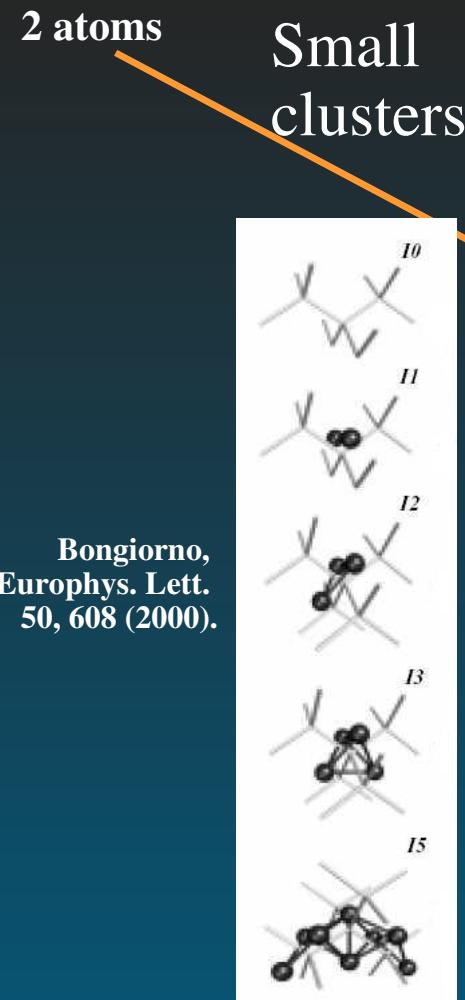


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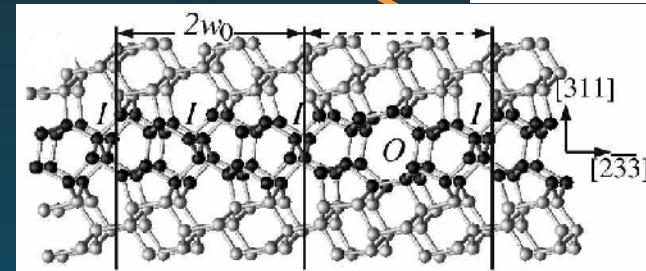
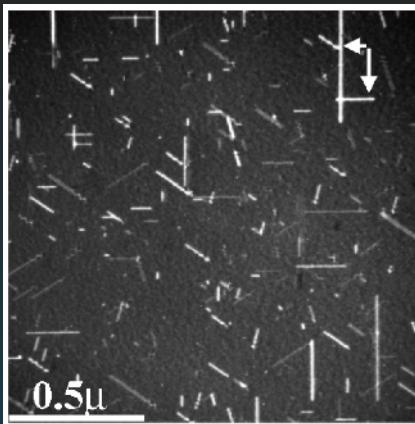


Extended defects

Role on extended defects formed after ion implantation of dopants

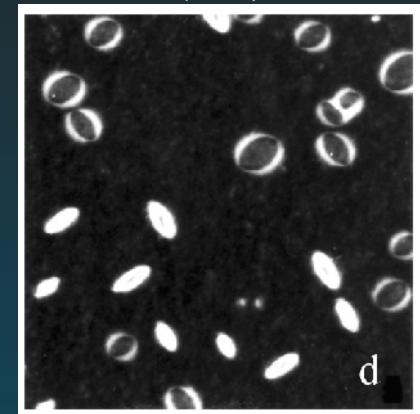


Cherkashin, MRS Symp. Proc. 810, C3.7 (2004).

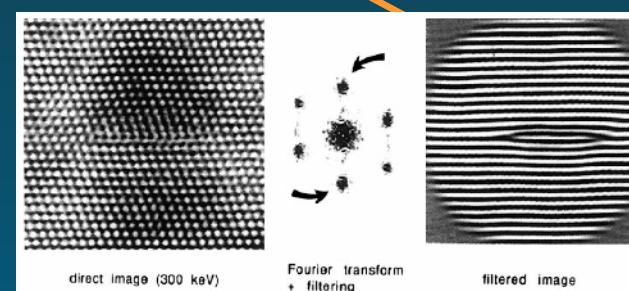


CEMES/LAAS

Claverie, MRS Symp. Proc. 610, B11.6 (2000).



Dislocation loops

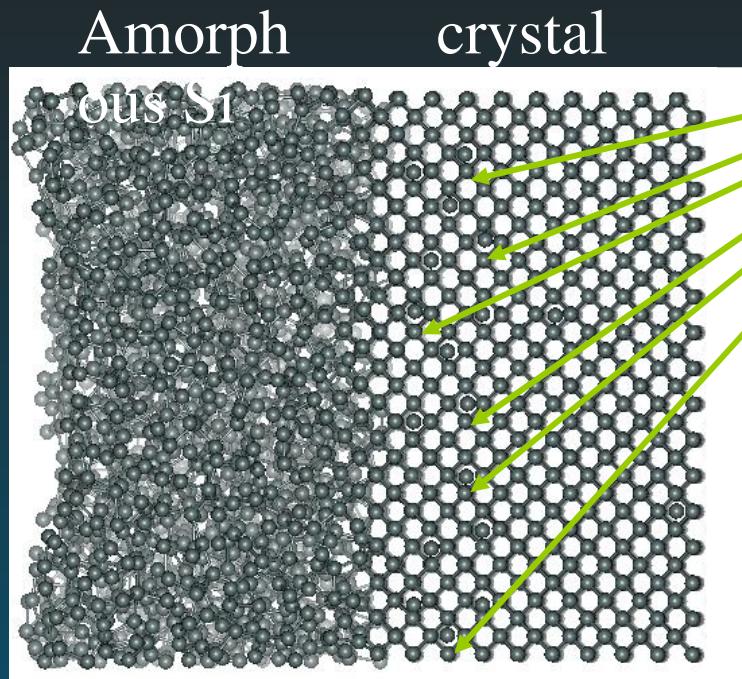


~ 10000 atoms

Boron Transient enhanced diffusion (TED) & extended defects

→ Common origin : the supersaturation of interstitials formed by the implantation step

Ex in the case of a preamorphisation :



Excess or supersaturation of interstitials just behind the amorphous /cristalline interface

Precipitation into extended defects

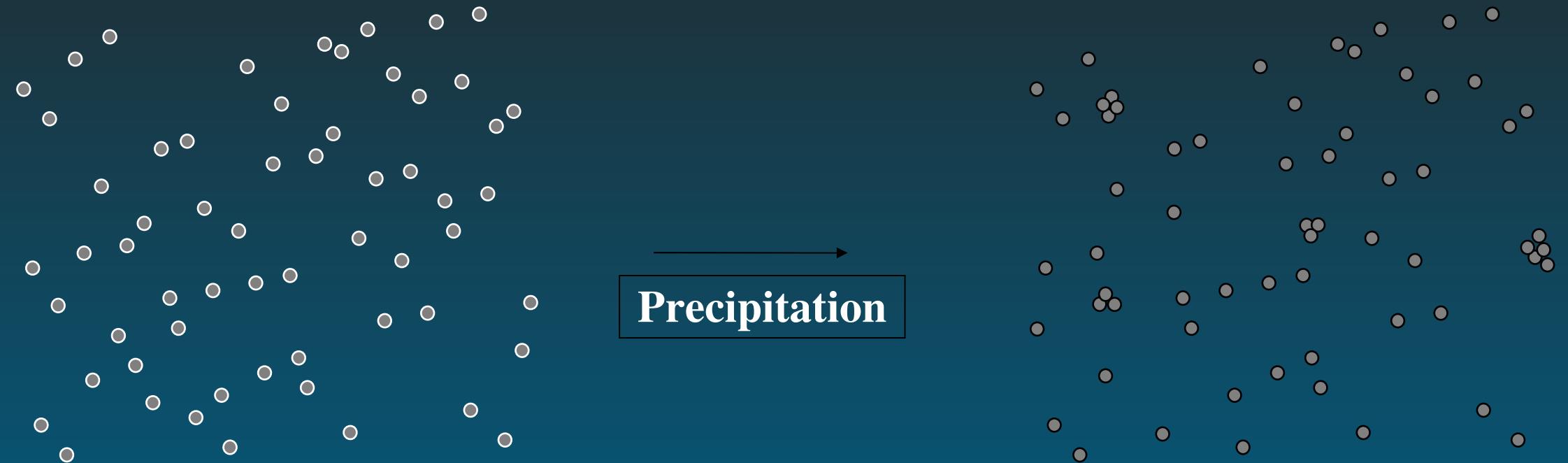
During annealing :

Accelerated diffusion of boron

→ Need to couple a model of extended defects to conventional packages of dopant diffusion

nucleation, pure growth and Ostwald ripening of defects

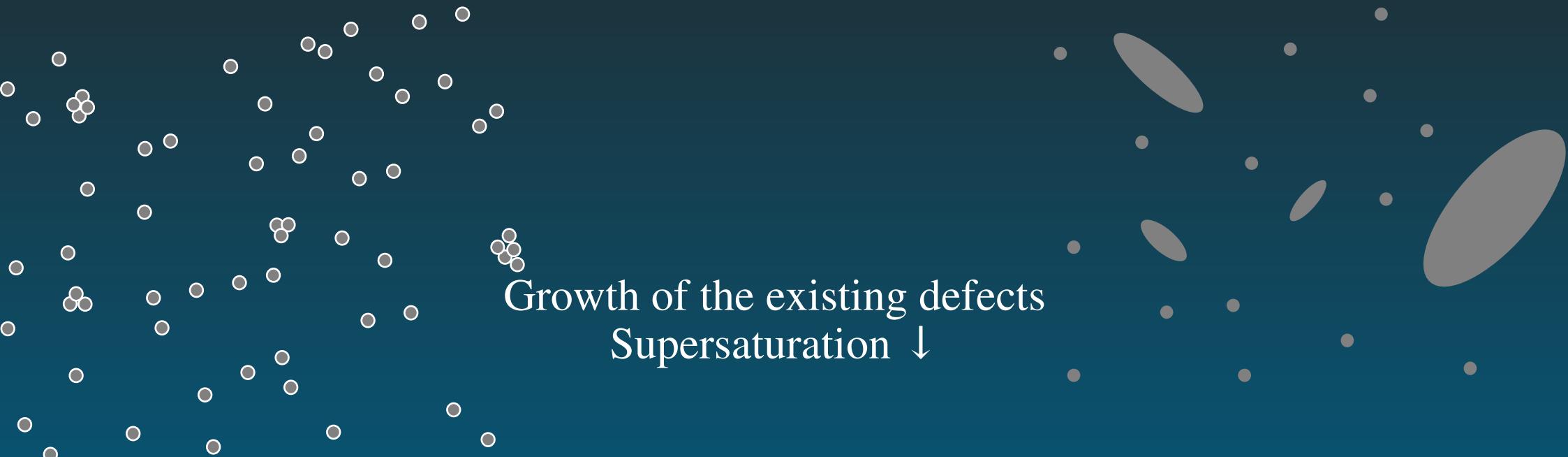
- Nucleation of extended defects – reduction of the system energy



nucleation, pure growth and Ostwald ripening of defects

- Nucleation of extended defects – reduction of the system energy
- Growth of the nuclei by absorption of the residual interstitials

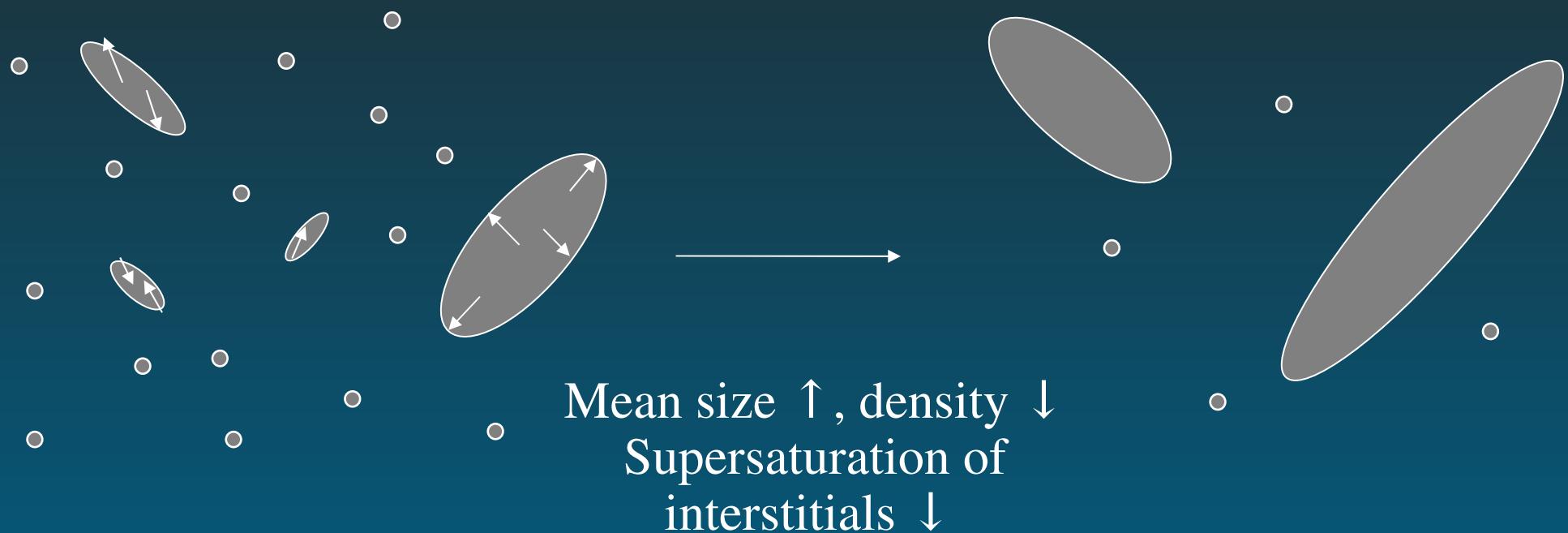
→pure growth



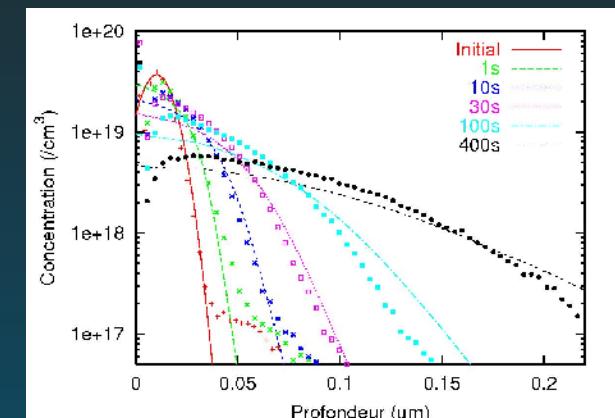
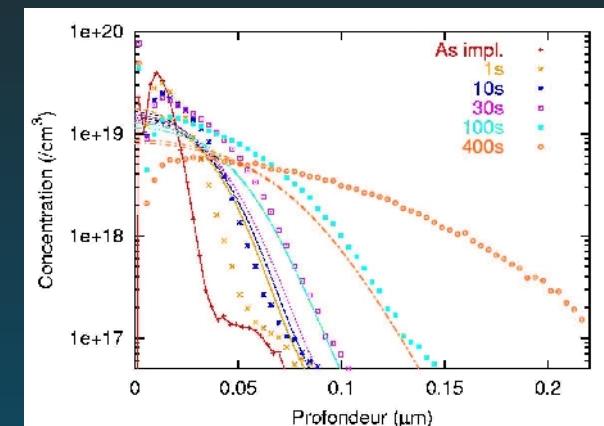
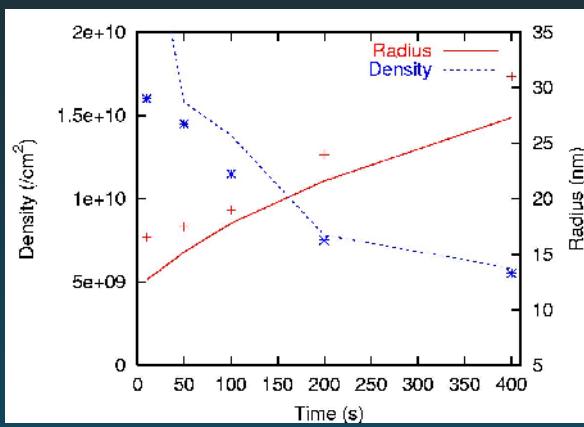
Growth of the existing defects
Supersaturation ↓

Nucleation, pure growth and Ostwald ripening of defects

- Nucleation of extended defects – reduction of the system energy
- Growth of the nuclei by absorption of the residual interstitials
 - pure growth
- Ostwald ripening (dynamical equilibrium) extended defects \leftrightarrow interstitial supersaturation



TED and Dislocation Loops (DL)



Evolution of density and size of Dislocations loops (DL)

Final TED diffusion effects underestimated if DL not considered

Good predictivity of TED effects with the incorporation of DL and Si interstitials evolution

Atom-by-atom model of defects evolution

Appl. Phys. A 76, 1025–1033 (2003)
 DOI: 10.1007/s00339-002-1944-0

Applied Physics A
 Materials Science & Processing

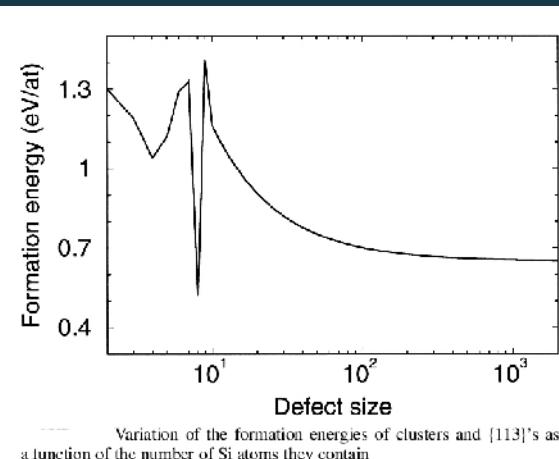
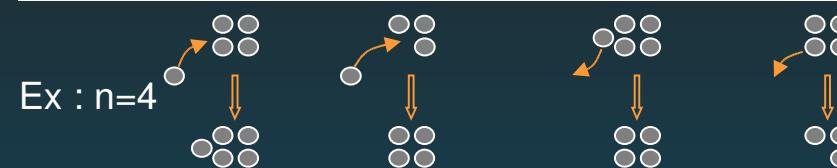
A. CLAVERIE^{1,*}
 B. COLOMBEAU¹
 B. DE MAUDUIT¹
 C. BONAFOS¹
 X. HEBRAS^{1,2}
 G. BEN ASSAYAG¹
 F. CRISTIANO²

Extended defects in shallow implants

¹ Ion Implantation Group CNRS Toulouse, CEMES/CNRS, BP 4347, 31055 Toulouse Cedex, France

² Ion Implantation Group CNRS Toulouse, LAAS/CNRS, 7 Ave. Colonel Roche, 31055 Toulouse Cedex, France

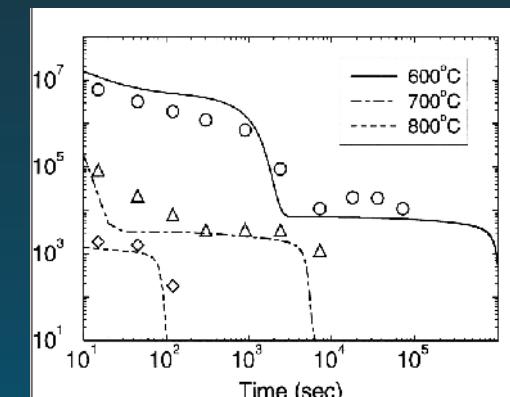
$$\frac{dN_n}{dt} = -[F_n N_n - F_{n-1} N_{n-1}] + R_{n+1} N_{n+1} - R_n N_n$$



Formation energies for clusters,
 {113}'s Cowern et al.

A. Claverie et al., Appl. Phys. A, Vol. 76, 2003 (Frendtech results)

Dissolution of {113}'s



Evolution of Si interstitials as a function of the time



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Coupling atom-by-atom model & diffusion

JOURNAL OF APPLIED PHYSICS

VOLUME 94, NUMBER 12

15 DECEMBER 2003

Prediction of boron transient enhanced diffusion through the atom-by-atom modeling of extended defects

E. Lampin^{a)}

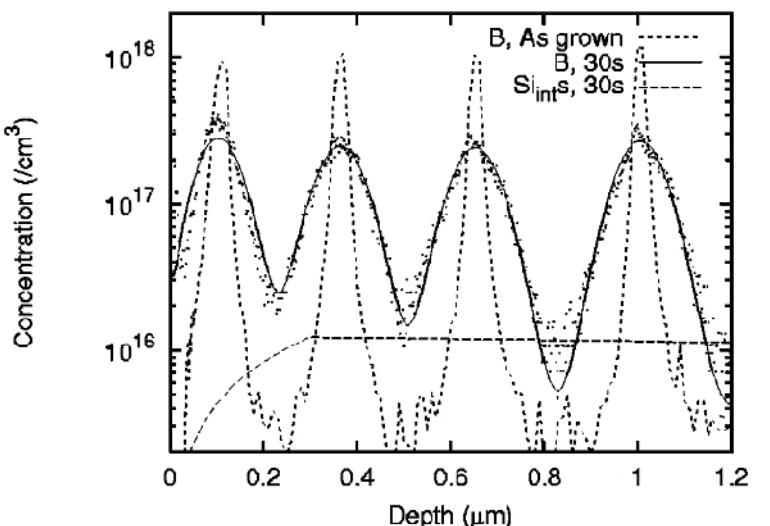
IEMN/ISEN, UMR CNRS 8520, 59652 Villeneuve d'Ascq, Cedex, France

F. Cristiano, Y. Lamrani, and A. Claverie

Ion Implantation Group, CEMES/I.AS-CNRS, 31055 Toulouse, France

B. Colombeau and N. E. B. Cowern

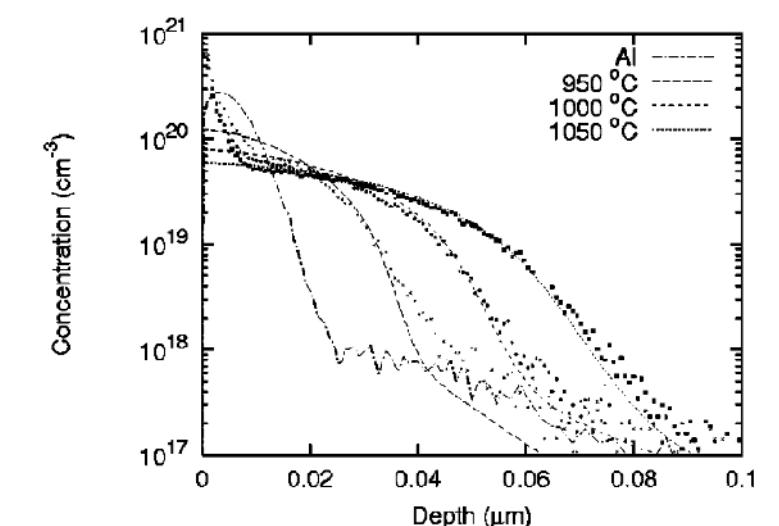
Advanced Technology Institute, University of Surrey, Guildford, GU2 7XH Surrey, United Kingdom



Nice simulation of TED effects
for marked layers experiments

However, simplified model for
Sprocess needed

E. Lampin et al., J. App. Phys., Vol 94, n°12, 2003 (Frendtech results)



Nice simulation of TED for
ultra-low Energy B+ implant



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Advanced annealing schemes

On a Computationally Efficient Approach to Boron-Interstitial Clustering

Johann Schermer and Peter Pichler

Fraunhofer-Institute of Integrated Systems and
Device Technology, Erlangen, Germany

Christoph Zechner

Synopsys Switzerland LLC
Zurich, Switzerland

Wilfried Lerch and Silke Paul

Mattson Thermal Products GmbH
Dornstadt, Germany

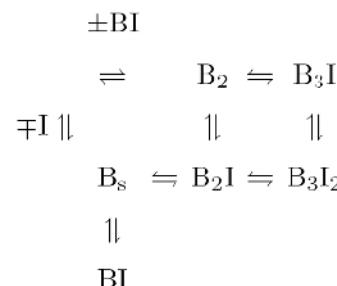


Figure 1: Scheme of reactions for the BICs model

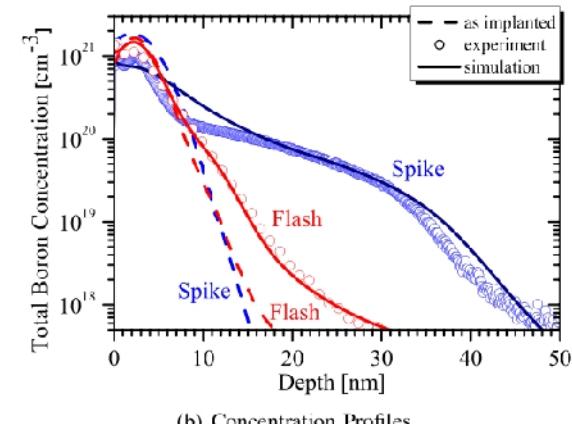
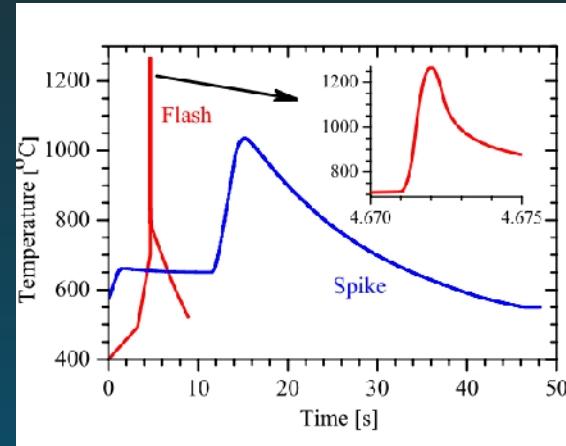
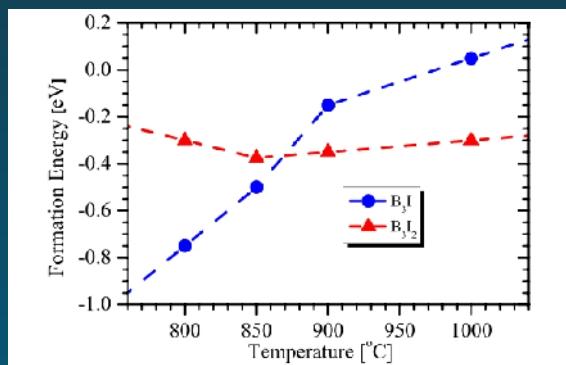


Fig. 8. Simulation results for Spike and Flash Anneal

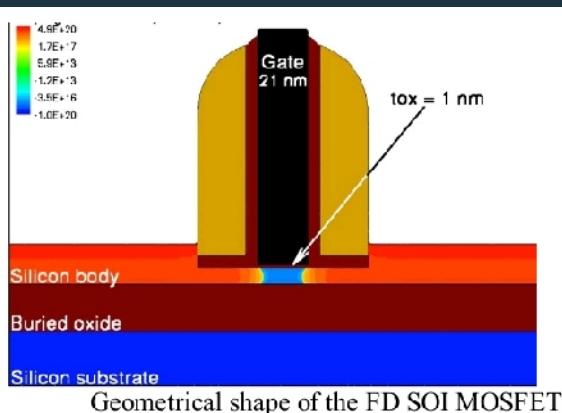
J. Shermer et al., ESSDERC 2007 (PULLNANO results)

Boron diffusion modeling & Device simulation

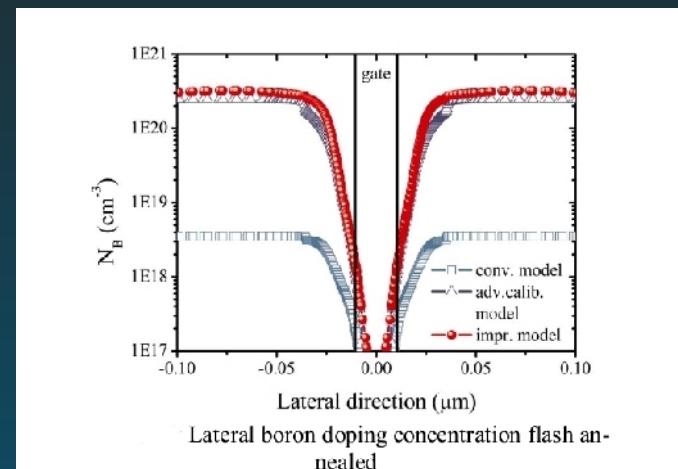
Process Models for Advanced Annealing Schemes and their Use in Device Simulation

P. Pichler^{1,2,*}, A. Martinez-Limia¹, C. Kampen¹, A. Burenkov¹, J. Schermer¹, S. Paul³, W. Lereh³, J. Gelpay⁴, S. McCoy⁴, H. Kheyrandish⁵, A. Pakfar⁶, C. Tavernier⁶, D. Bolze⁷

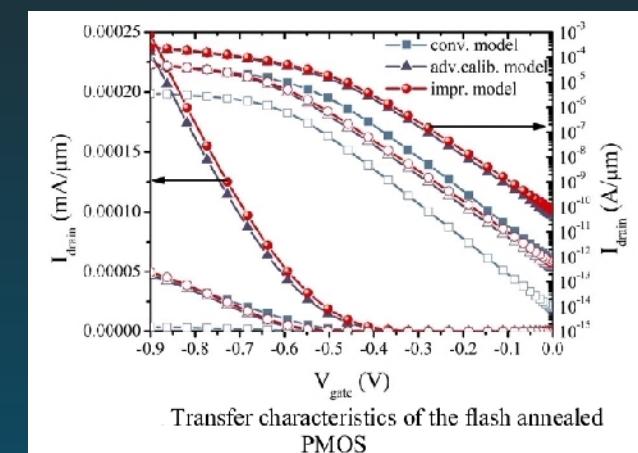
¹Fraunhofer-Institute of Integrated Systems and Device Technology (IISB),
Schottkystrasse 10, 91058 Erlangen, Germany



FD nanometric SOI device



Impact of the diffusion modeling on the boron profile



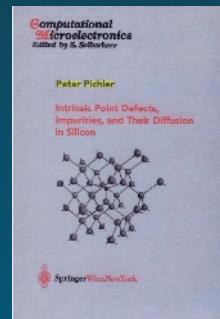
Large impact on the PMOS electrical characteristic predicted

P. Pichler et al., International Workshop on junction Technology (2008), ATOMICS & PULLNANO Results



Conclusion

- Large progress have been done in junction processing modeling in the framework of several european projects (Rapid, Frendtech, Pullnano, Atomics) with the collaboration of Synopsys (Zurich)
- Some of the models presented (simplified form) in Sentaurus Process or script transfered to semiconductor compagnies
- But still a lot of work:
 - Influence of stress effects
 - New Material (SiGe S/D, Ge....)
 - Advanced annealing scheme (laser annealing, solid phase epitaxy)
- More information :



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Part V (prospective)

Atomistic TCAD : towards some computer experiment ?

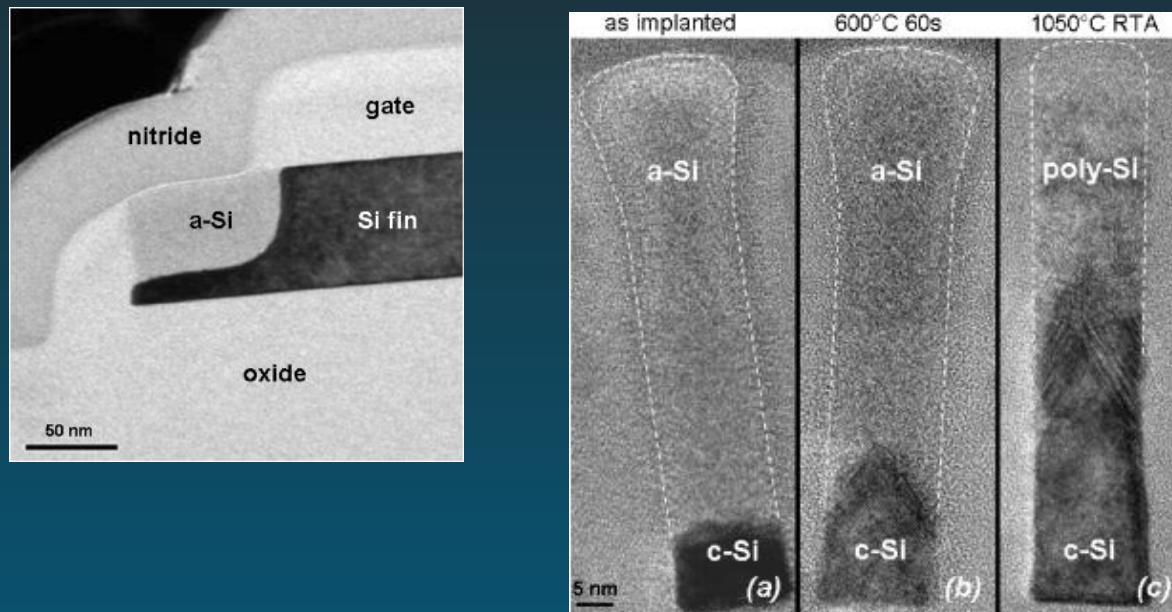
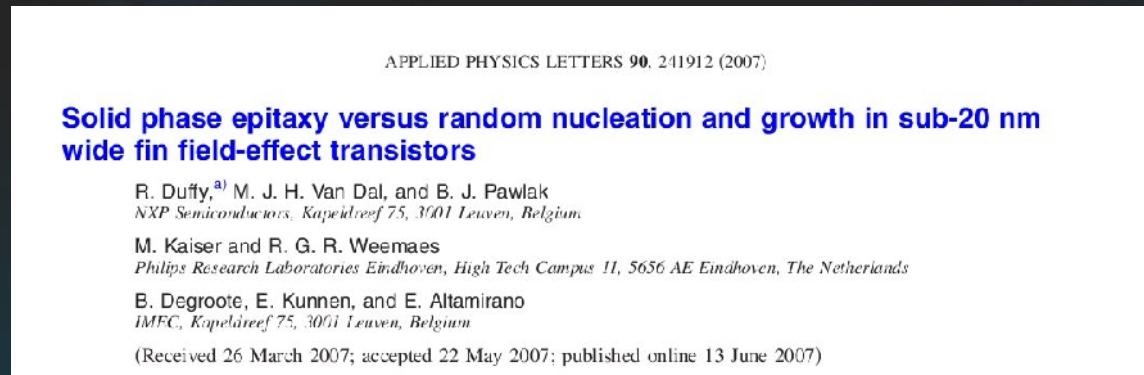


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Complexity & Limits of a full experimental optimisation (1) ?

- Complex integration in nanodevices



(PULLNANO results)

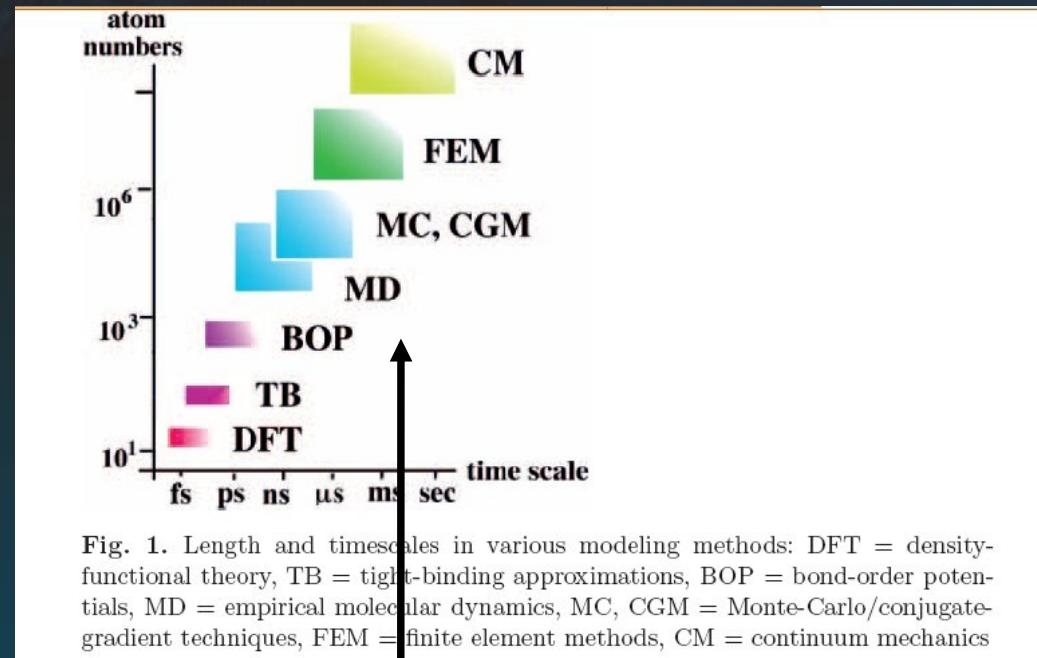
Complexity & Limits of a full experimental optimisation (2) ?

How to characterise diffusion mechanism during a solid phase epitaxy when Time/Temperature window available reduced by recrystallisation ?



- A solution proposed by Venezia et al.: Diffusion in completely amorphised silicon layer (but the influence of recrystallisation is not taken into account)
- Computer experiment (Atomistic TCAD) needed but it will not replace standard TCAD !

Which method for computer experiment ?



[Scheerschmidt07] http://www.mpi-halle.de/mpi/publi/pdf/6735_06.pdf

Development of atomistic approach based
on molecular dynamics (MD)

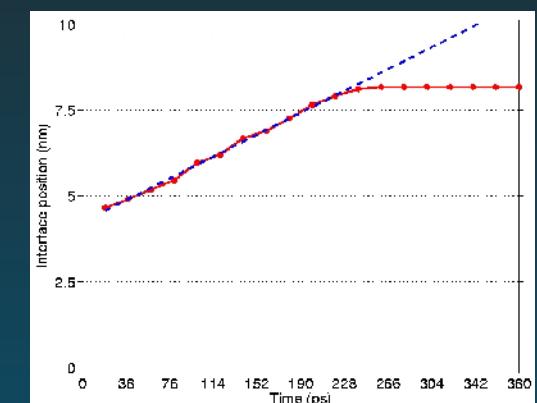
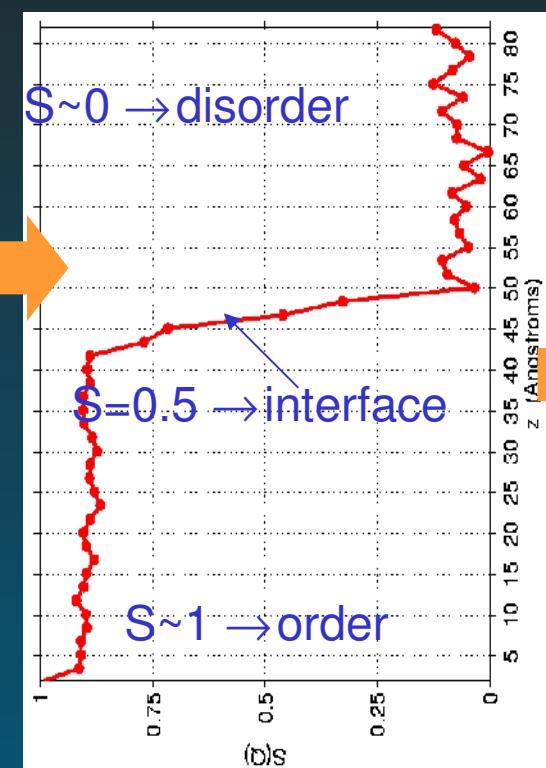
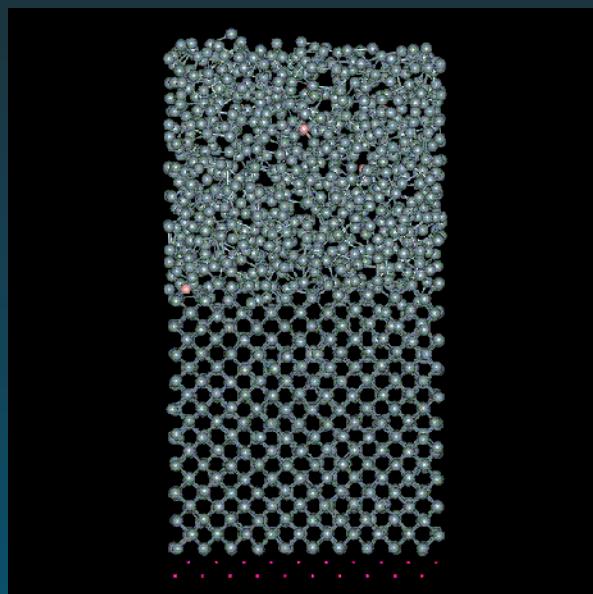
Molecular Dynamics of LPE, SPE regrowth

Simulation of the annealing and exploitation

Example of annealing, Stillinger-Weber, 1200 K

Extraction interface
from 1D structure factor

Procedure repeated to extract
the recrystallization velocity

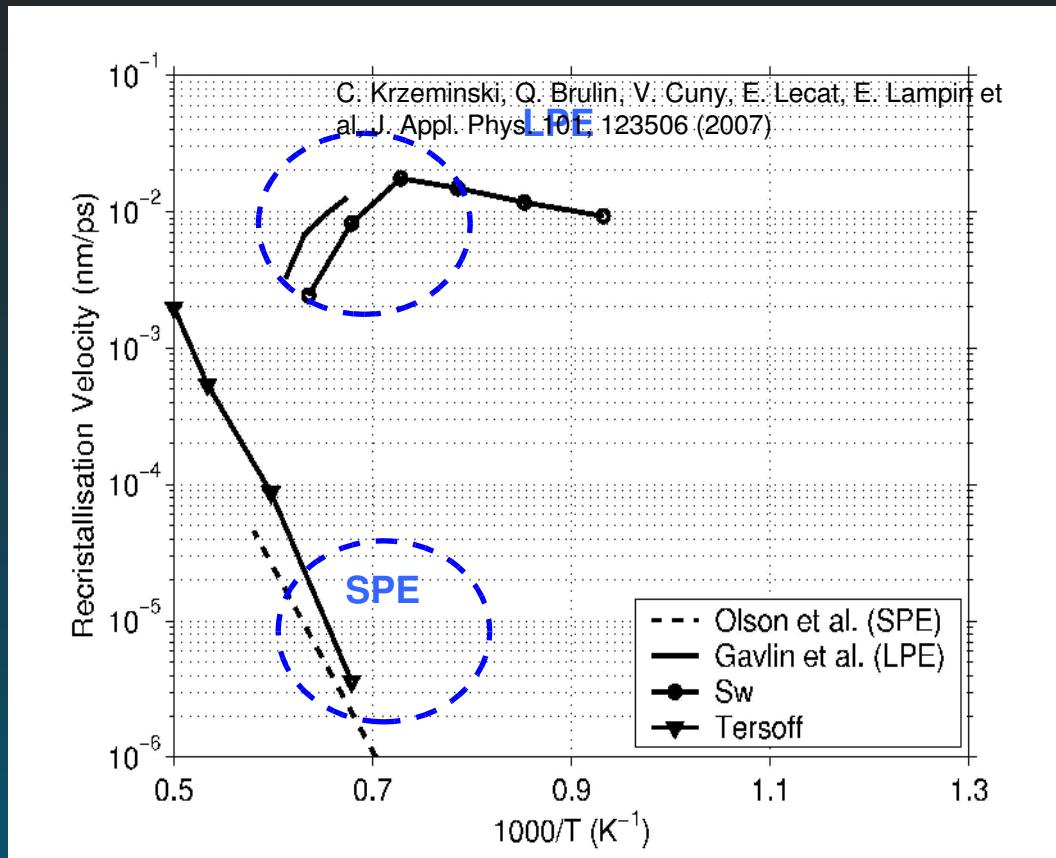


Extraction of the position of
the interface vs time

Molecular dynamics of SPE, LPE regrowth (2)

Conclusion :

Analysis of the velocities of recrystallization and of the structure of disordered part :



Potentiality to simulate both SPE and LPE

SPER or flash annealing

Laser annealing

(PULLNANO results)

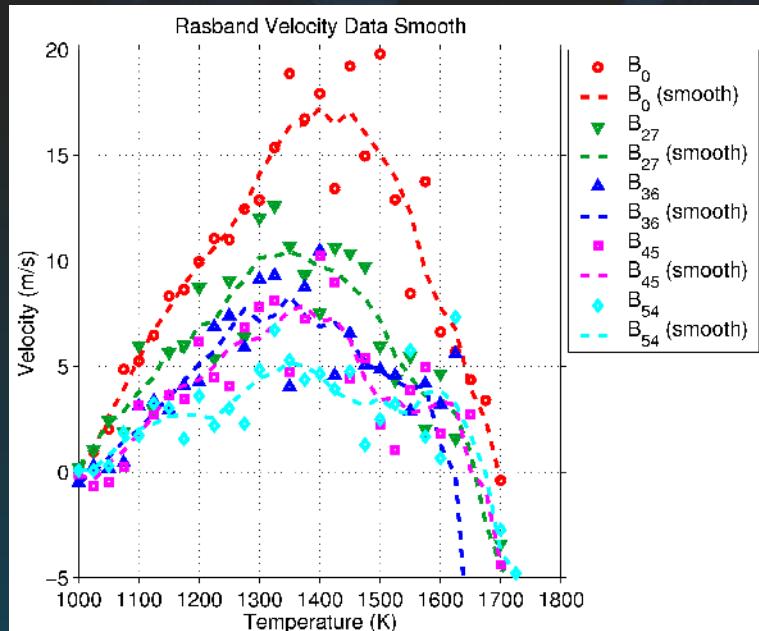


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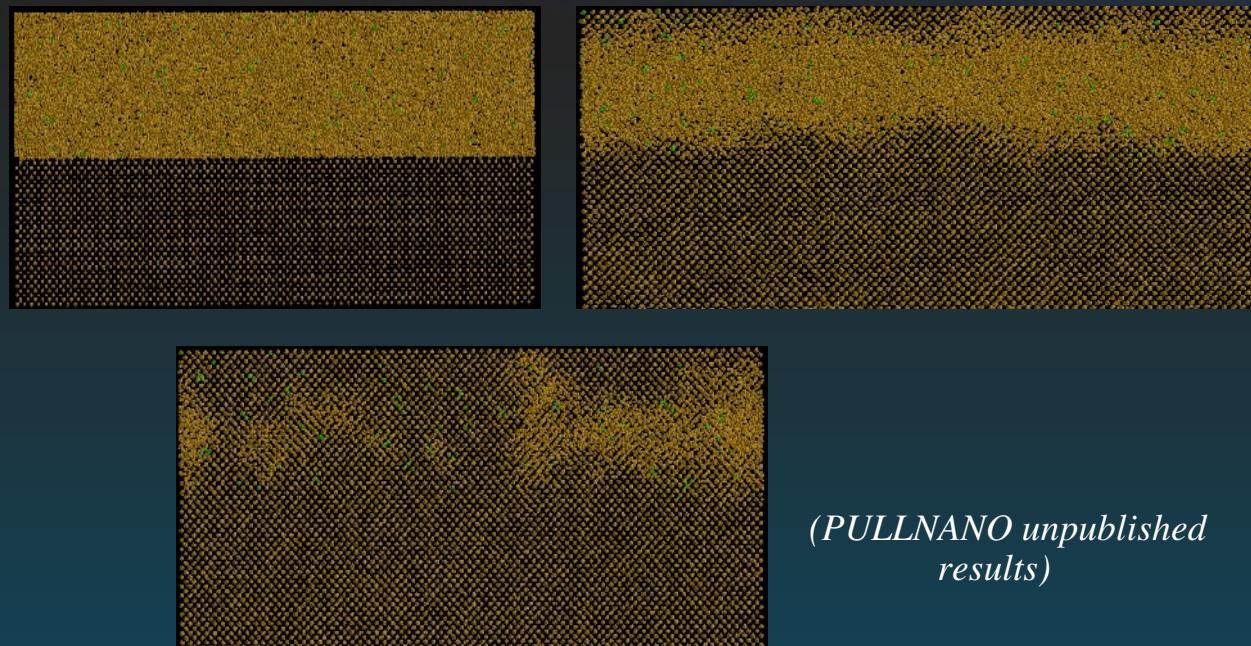


Boron doped LPE regrowth

Reduction of the velocity for large B concentration

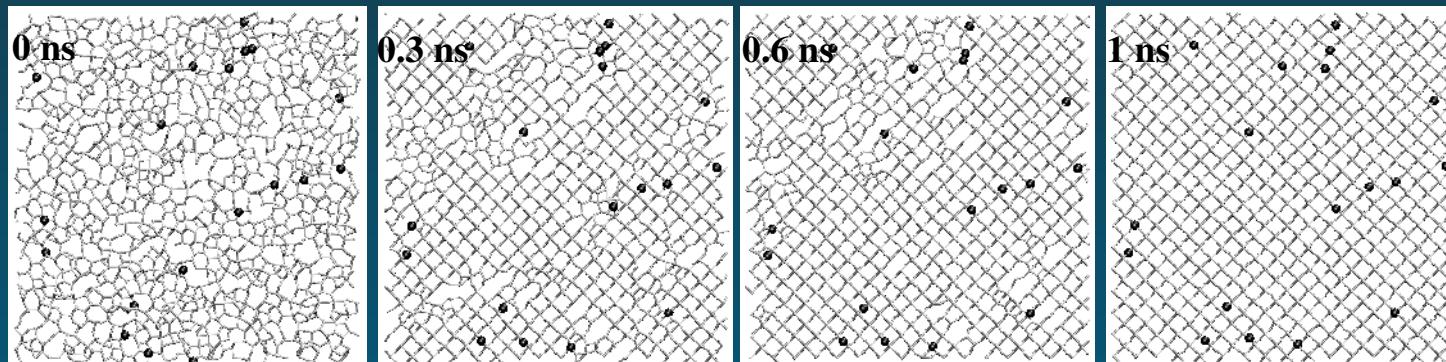


Interface roughening & amorphous pockets



(PULLNANO unpublished results)

Incorporation of boron atoms in c-Si

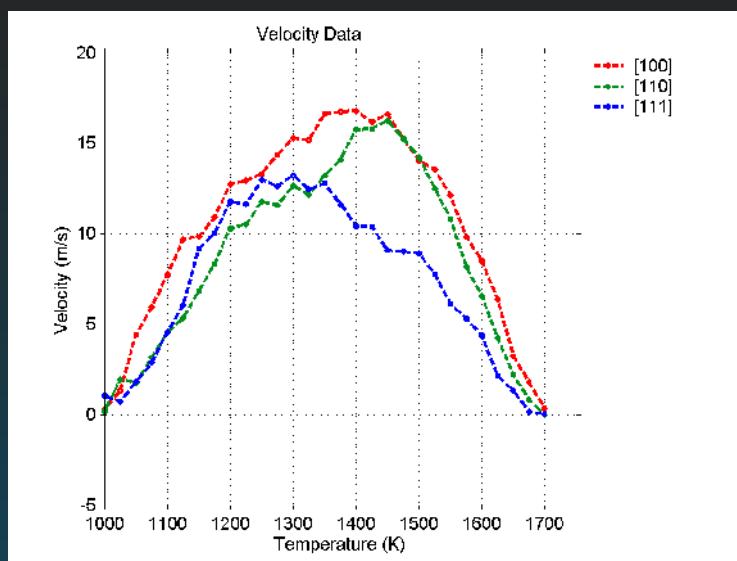


A. Mattoni and L. Colombo,
Phys. Rev. B 69 (2004) 045204

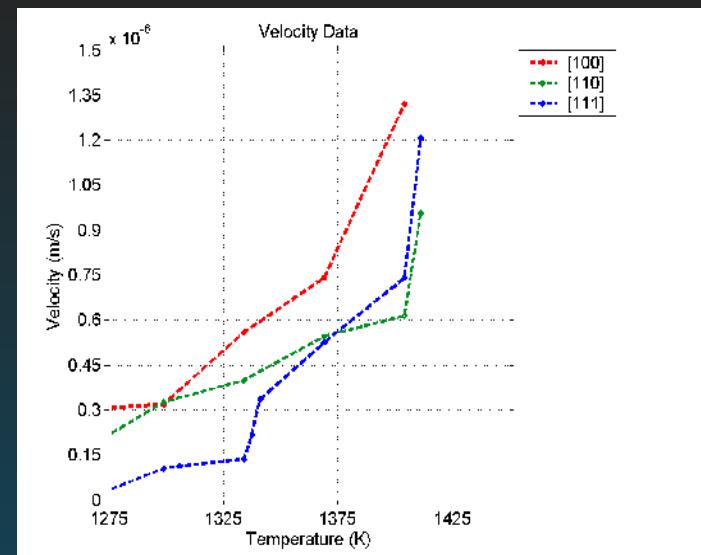
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LPE or SPE: influence orientation effects



Orientation influence for LPE [100]>[110]>[111]



Orientation influence for SPE [100]>[110]>[111]

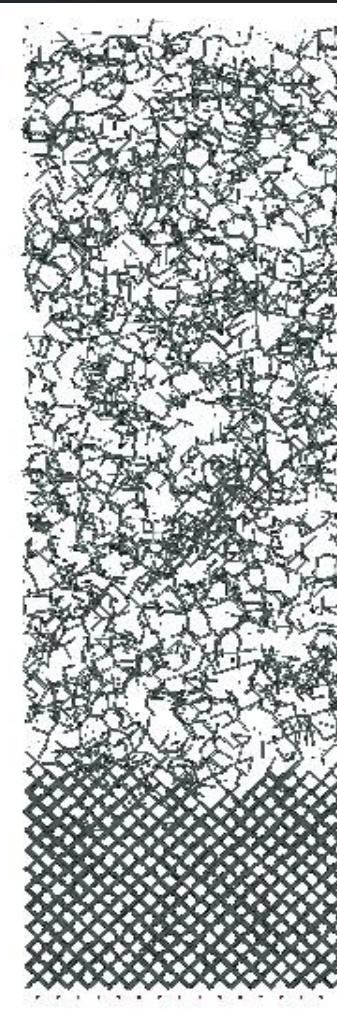
(PULLNANO unpublished results)

Competition SPE/RNG

Thick
amorphous layer



Thin crystalline germ

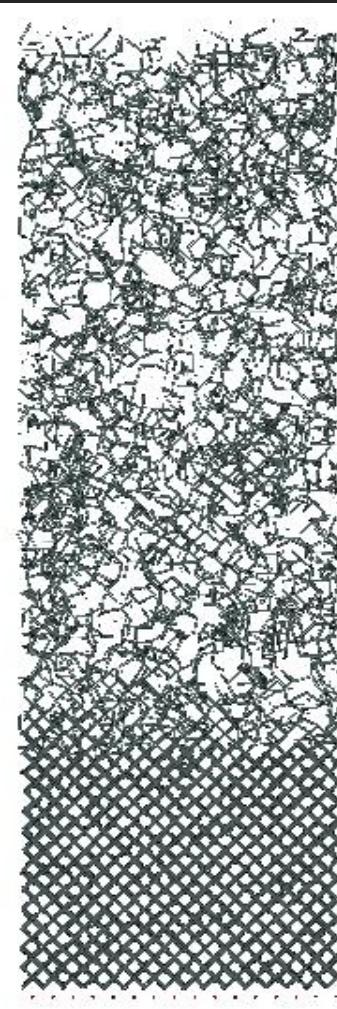


30 ns

(PULLNANO unpublished results)

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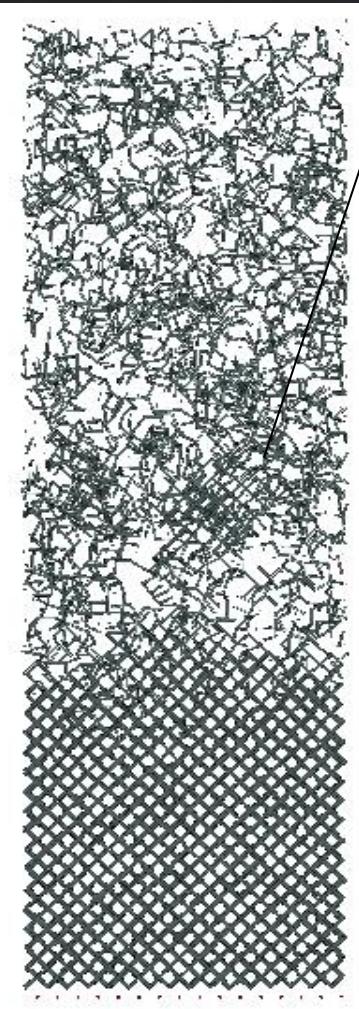
Some grains begin to form
by RNG



60 ns



80 ns



Crystallization has
progressed by SPE

